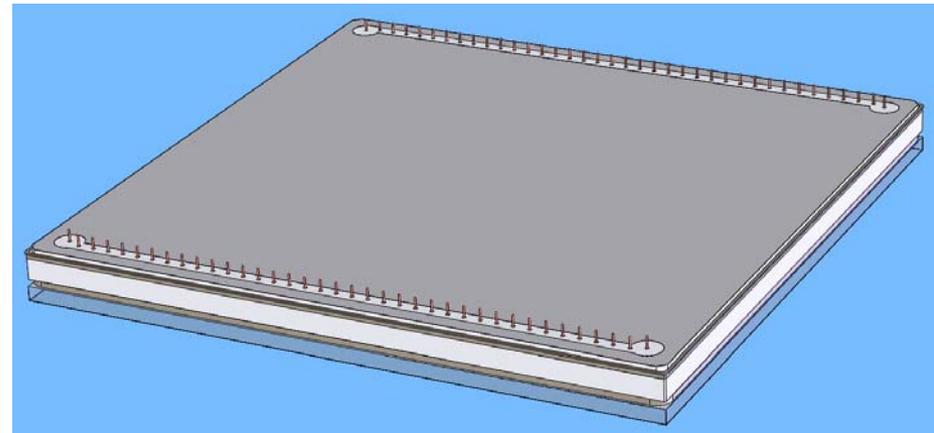
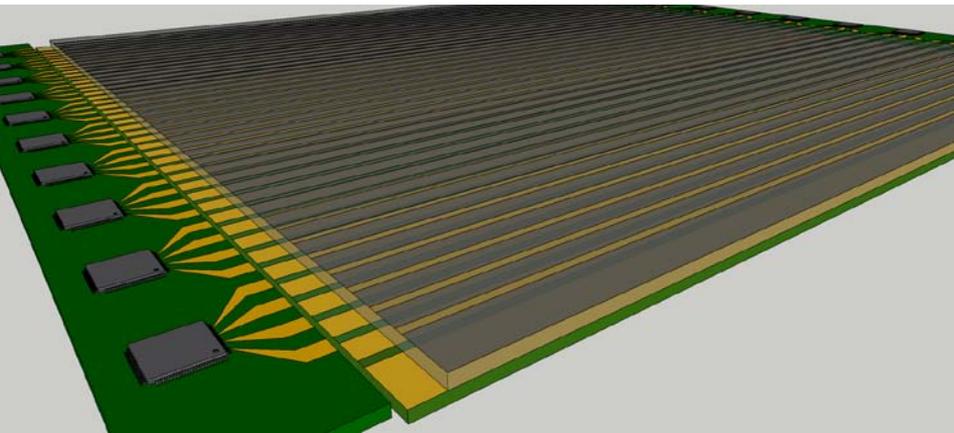


8" ceramic MCP-PMT Readout

Status Update

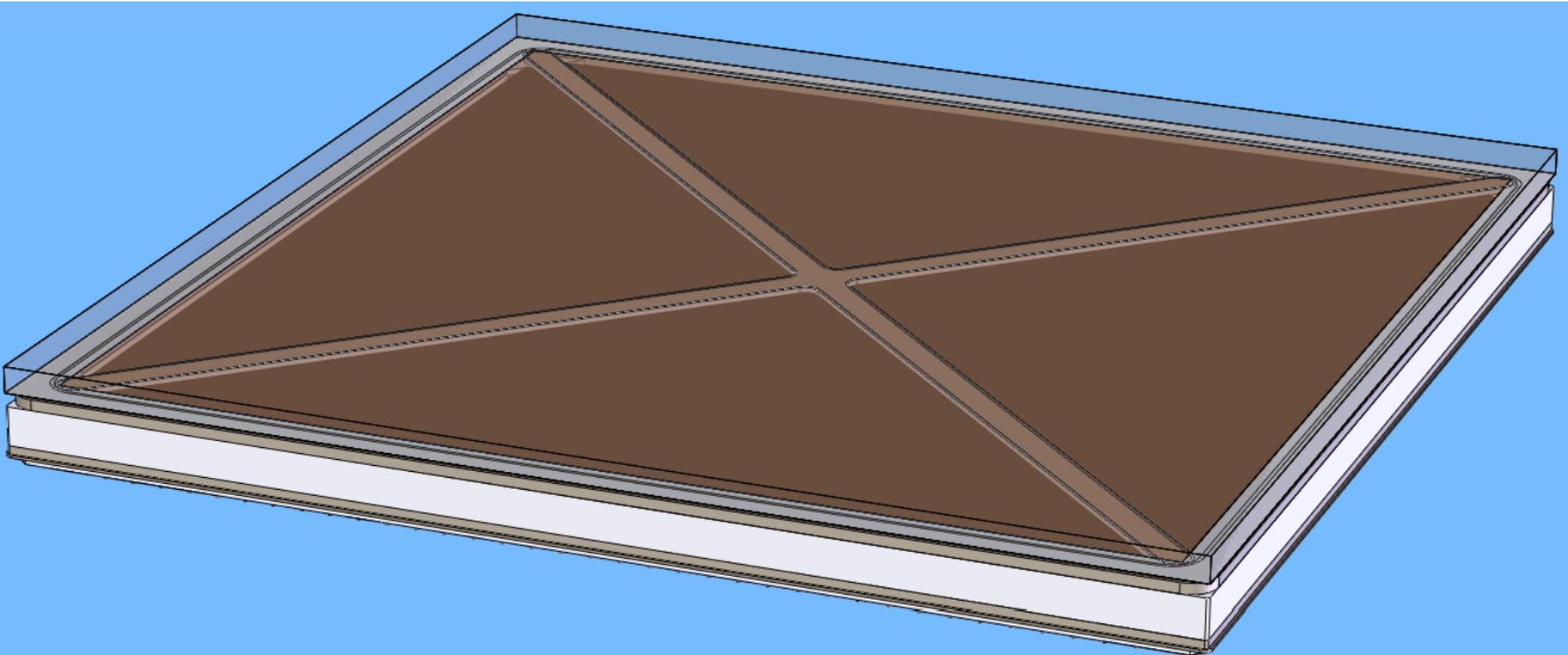
Matt Andrew (Univ. of Hawaii)
for the LAPPD Electronics Group

9-JUL-2012 Electronics GPC Review



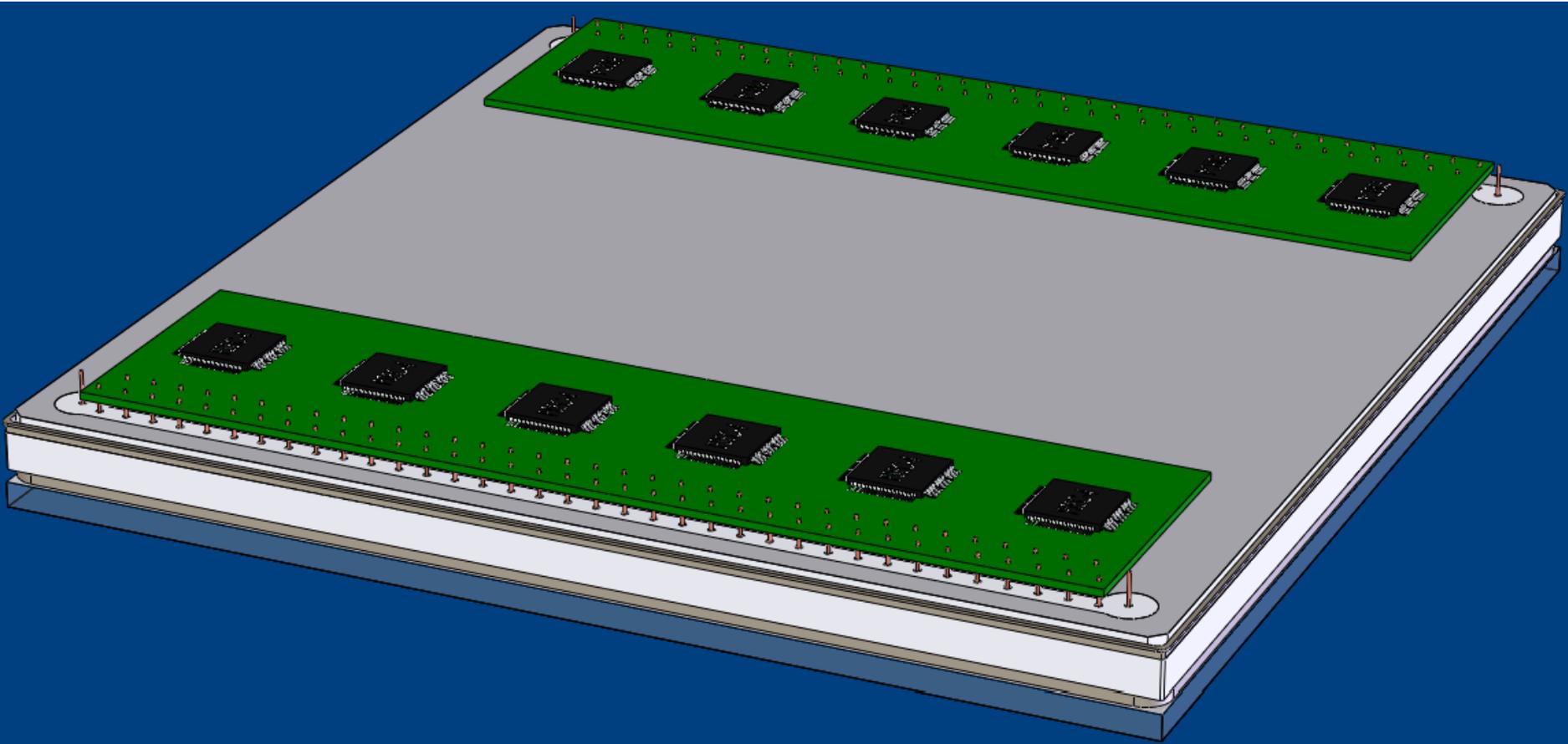
8" Ceramic PMT @ SSL

- **Baseline (strip-line to outside) design:**
 - 1. PSEC ASIC**
 - 2. Stripline readout**
 - 3. Digital / Central cards**
- **First ceramic functional articles:**



8" Ceramic PMT @ SSL

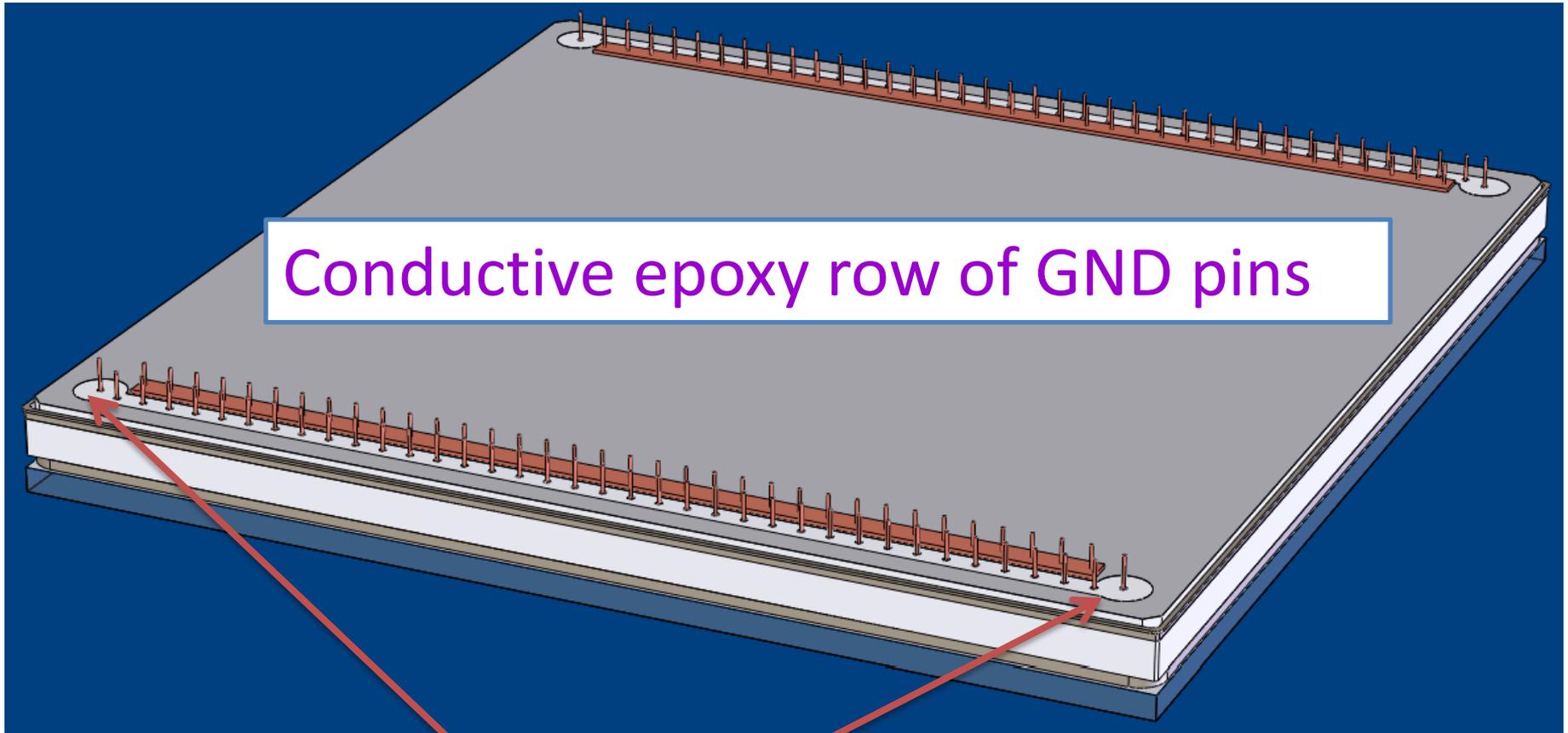
- Ceramic design
 1. Same Analog card ?



8" Ceramic PMT @ SSL

- Ceramic design

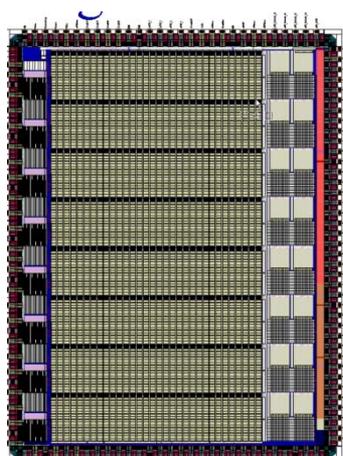
1. Same Analog card ? → too much stress



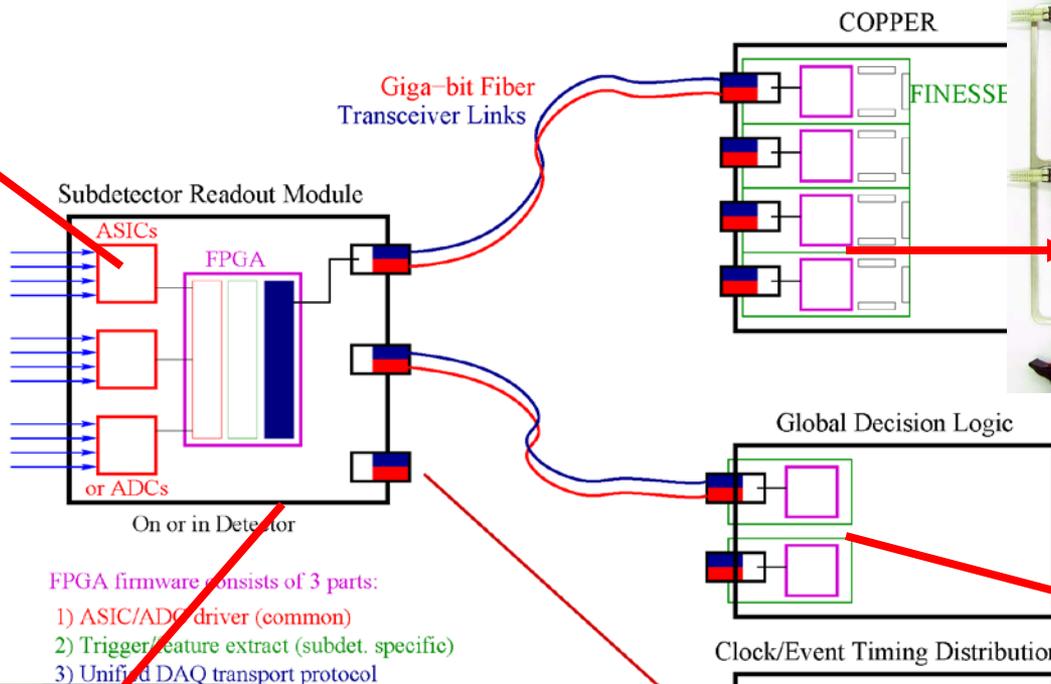
Conductive epoxy row of GND pins

Discrete pig-tail for HV pins

Leverage experience (Belle II)

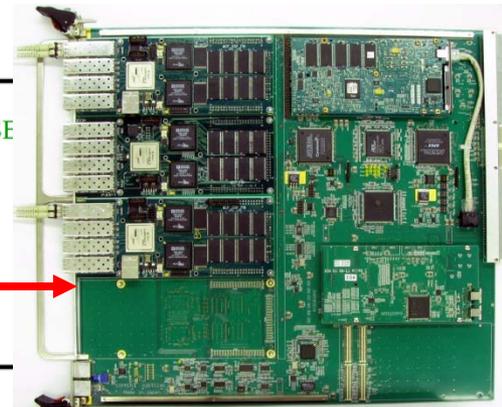
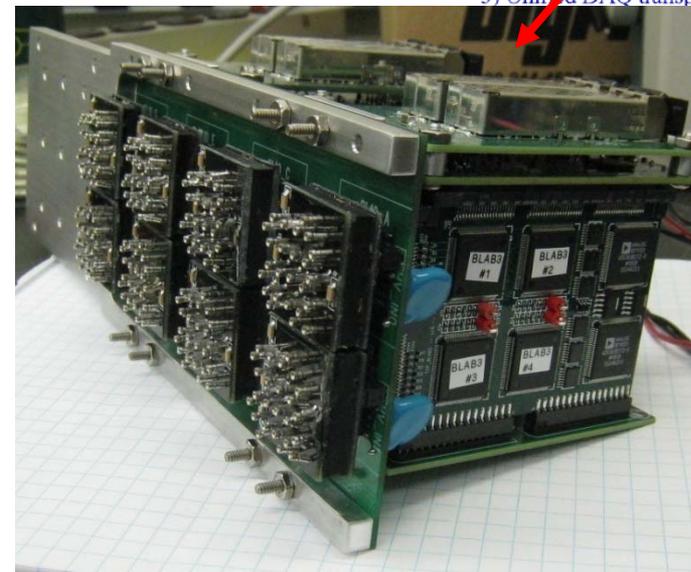


Third generation waveform sampling ASIC



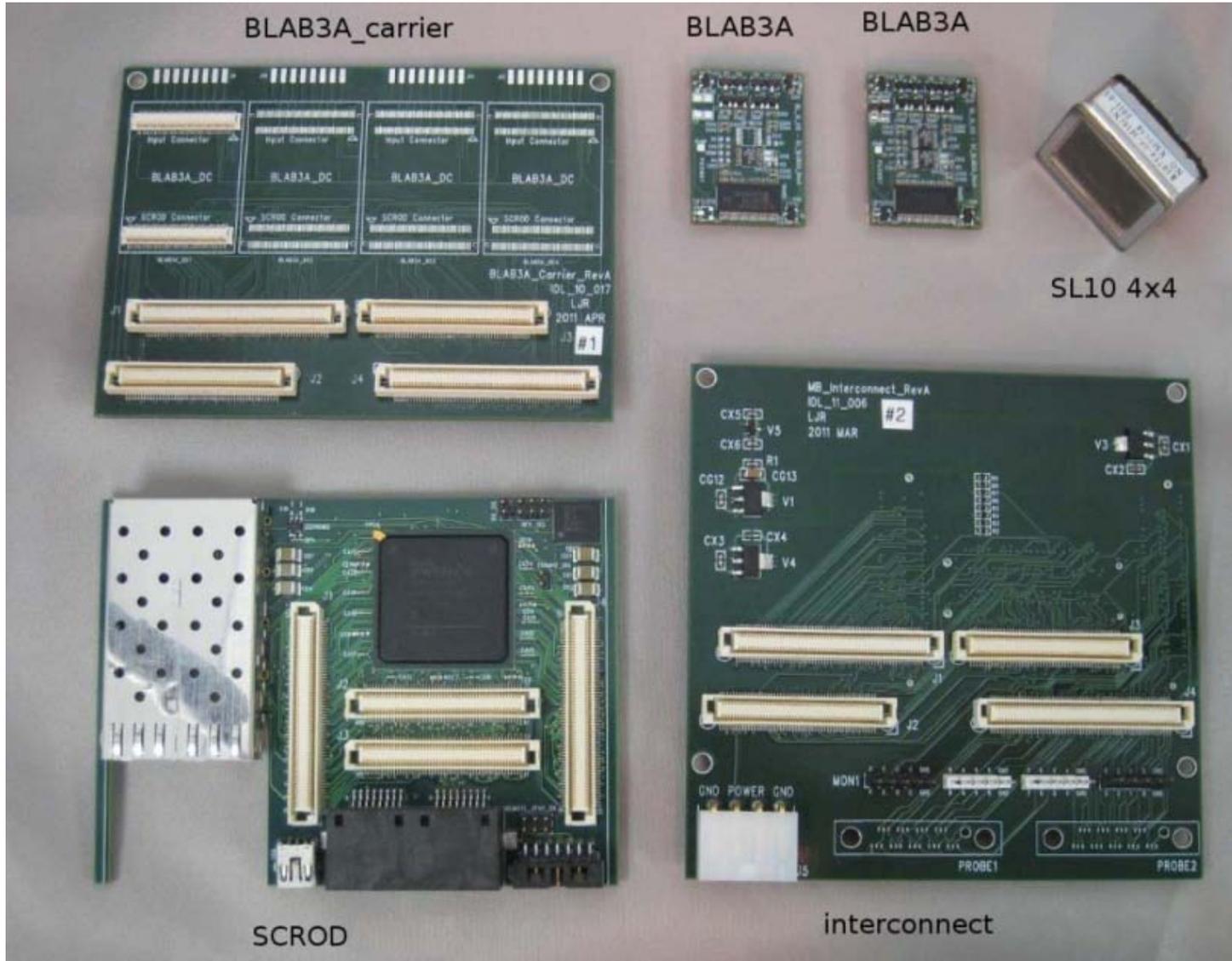
- FPGA firmware consists of 3 parts:
- 1) ASIC/ADC driver (common)
 - 2) Trigger feature extract (subdet. specific)
 - 3) Unified DAQ transport protocol

Clock jitter cleaners



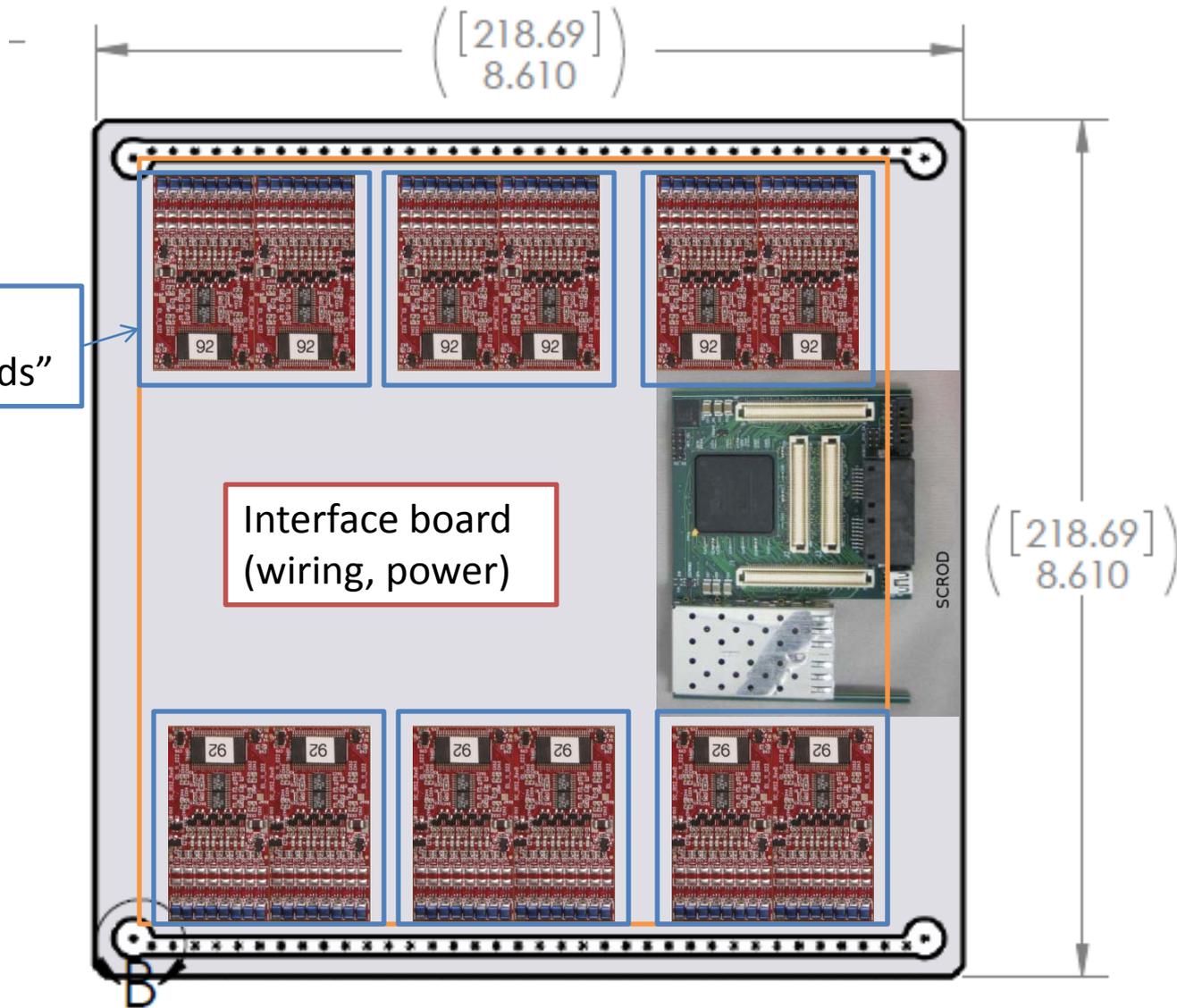
8" Ceramic PMT @ SSL

- Compact analog + digital card “stack”

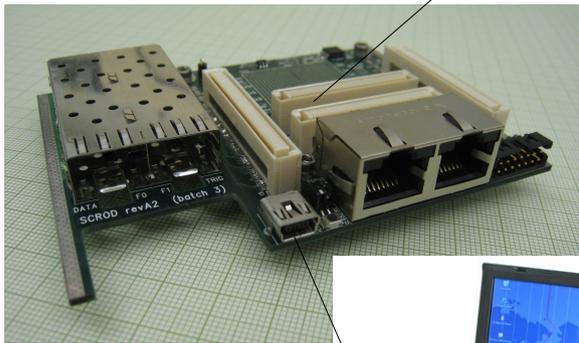
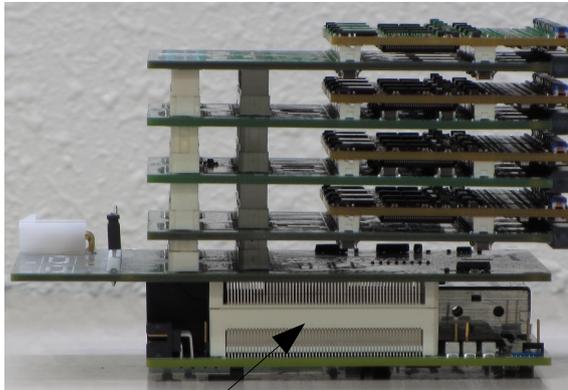


Dec. 2011 Concept

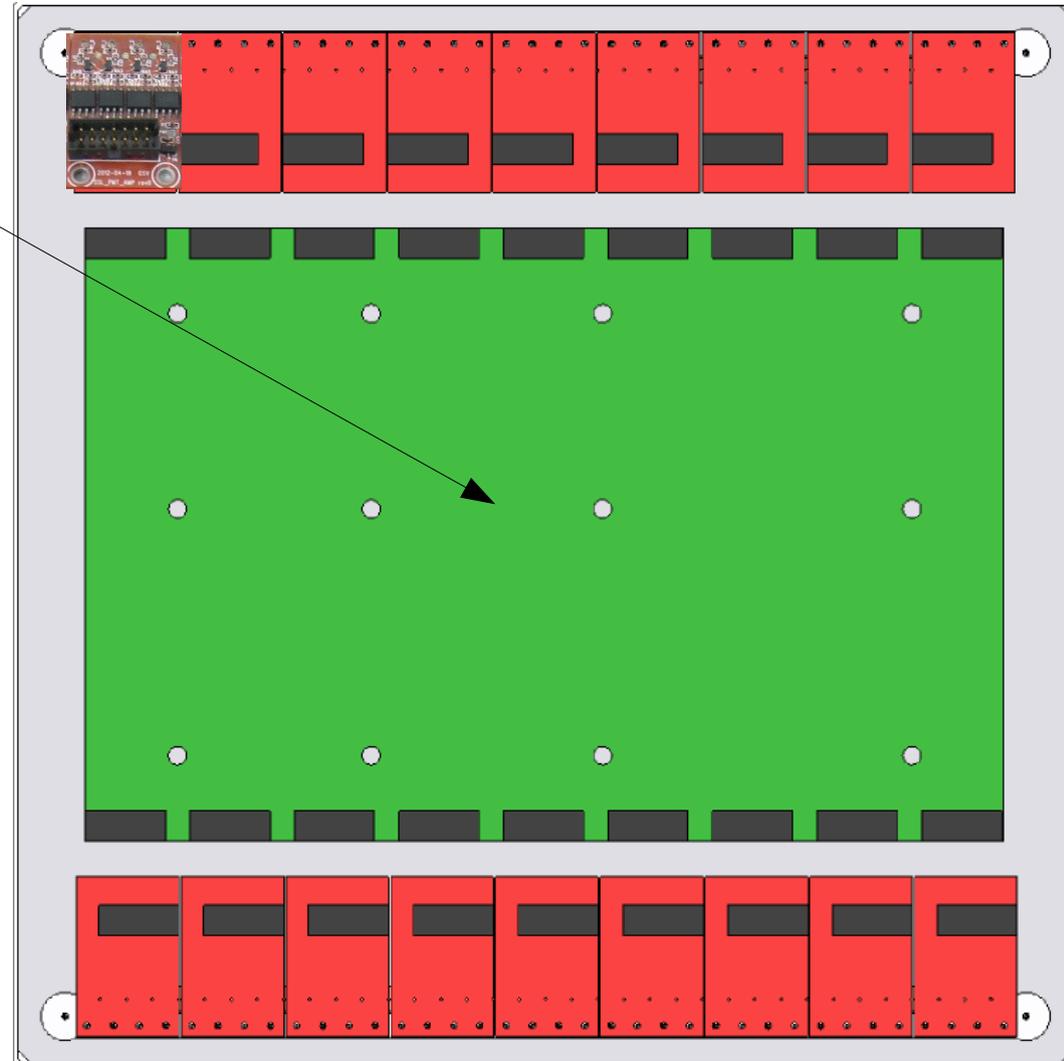
Different “interface” board



Readout Status for 8" Ceramic PMT



USB



- SSL_PMT_AMP and SSL_front boards fabricated and assembled
- New SCROD+new boardstack+new ASIC daughtercards in hand and functional
- USB readout firmware+software functional (still needs a little development)
- Firmware to self-trigger still needs to be written