

# Fast Tracker (FTK) Status

- **FTK system overview**
- **ANL commitment**
  - **Physics performance and system design**
  - **FTK-LVL2 Interface (FLIC)**
  - **Testbeds (vertical slice)**
  - **3D AM chip R&D**

**Jinlong Zhang**

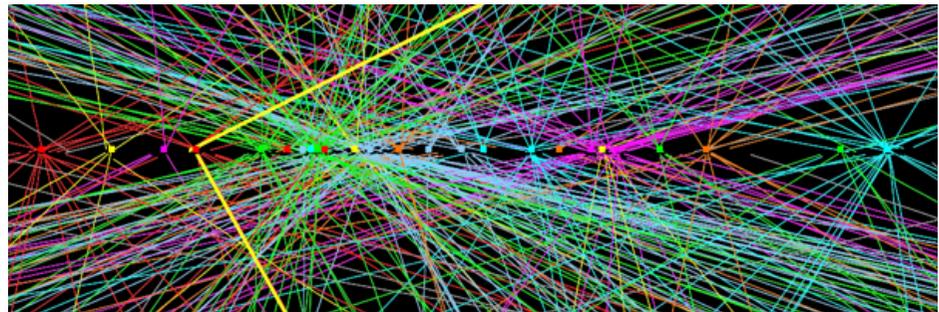
# FTK Team

- **Italy**
  - **Bologna, Ferrara, Frascati, Milano, Pavia, Pisa**
- **Japan**
  - **Waseda**
- **US**
  - **Argonne, Chicago, Fermilab, Illinois, Northern Illinois**



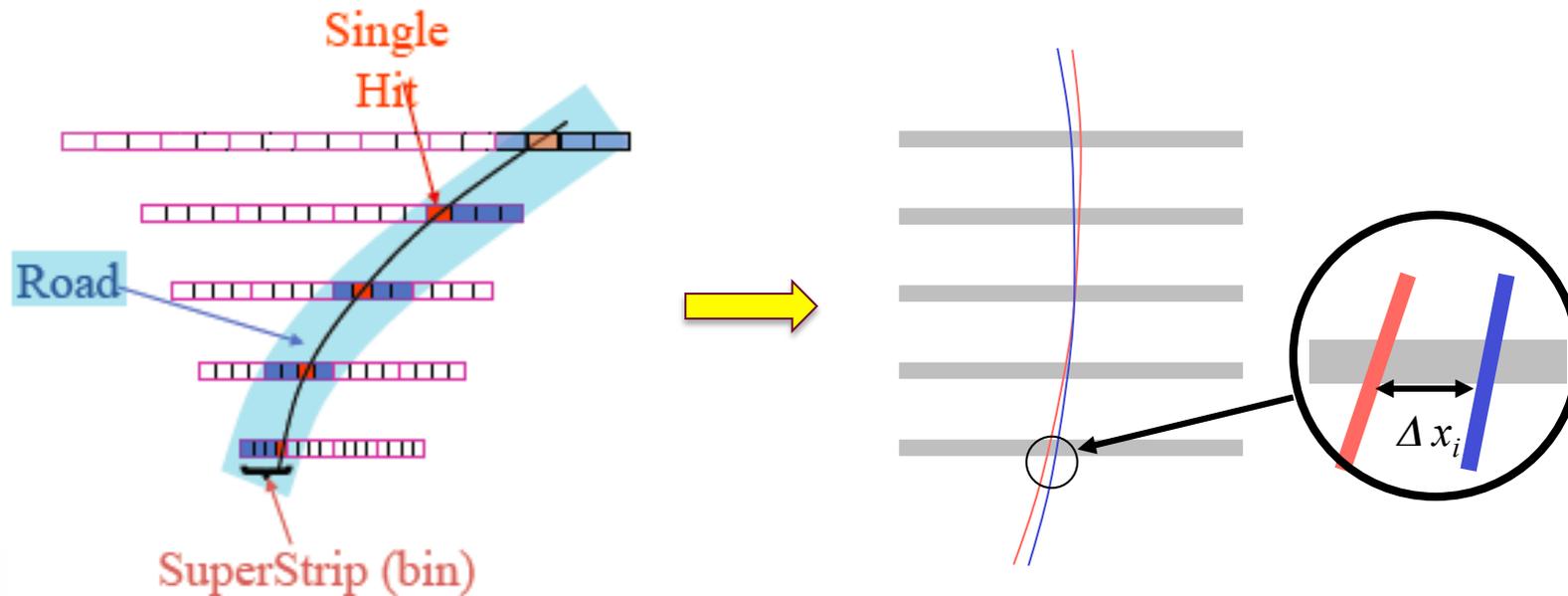
# Challenge & Solution

- **Capability to examine more event characteristics at the earlier trigger levels**
  - Tracking required for heavy flavor object (b-jets,  $\tau$ -jets) identification and lepton isolation
  - Large tracking execution time due to hit density and time consuming trigger algorithms due to backgrounds
- **A hardware track finder FTK**
  - Completing global tracking at the full L1A rate (100 KHz) and providing the full track list to the Level-2 trigger (LVL2) algorithms
  - Freeing up the LVL2 resource for sophisticated event selection algorithms



# FTK Approach

Use hardware to perform the global tracking in two steps  
 pattern recognition (in Associative Memory, AM) and track fit (in DSPs)



Pattern recognition in coarse resolution  
 (superstrip → road)

Track fit in full resolution (hits in a road)  
 $F(x_1, x_2, x_3, \dots) \sim a_0 + a_1 \Delta x_1 + a_2 \Delta x_2 + a_3 \Delta x_3 + \dots = 0$

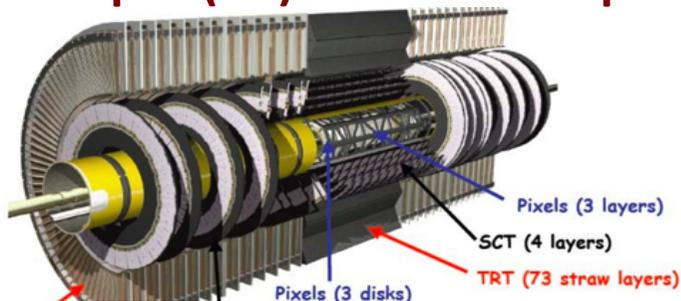
Road size to balance the workload between two steps

Prestored patterns ( $10^9$ )

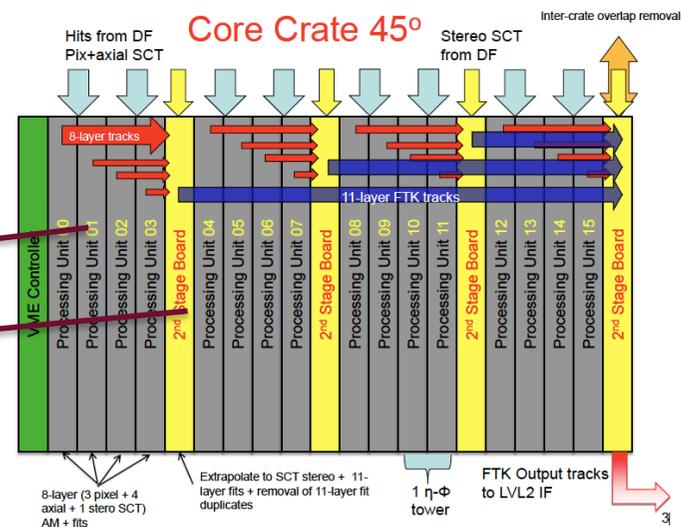
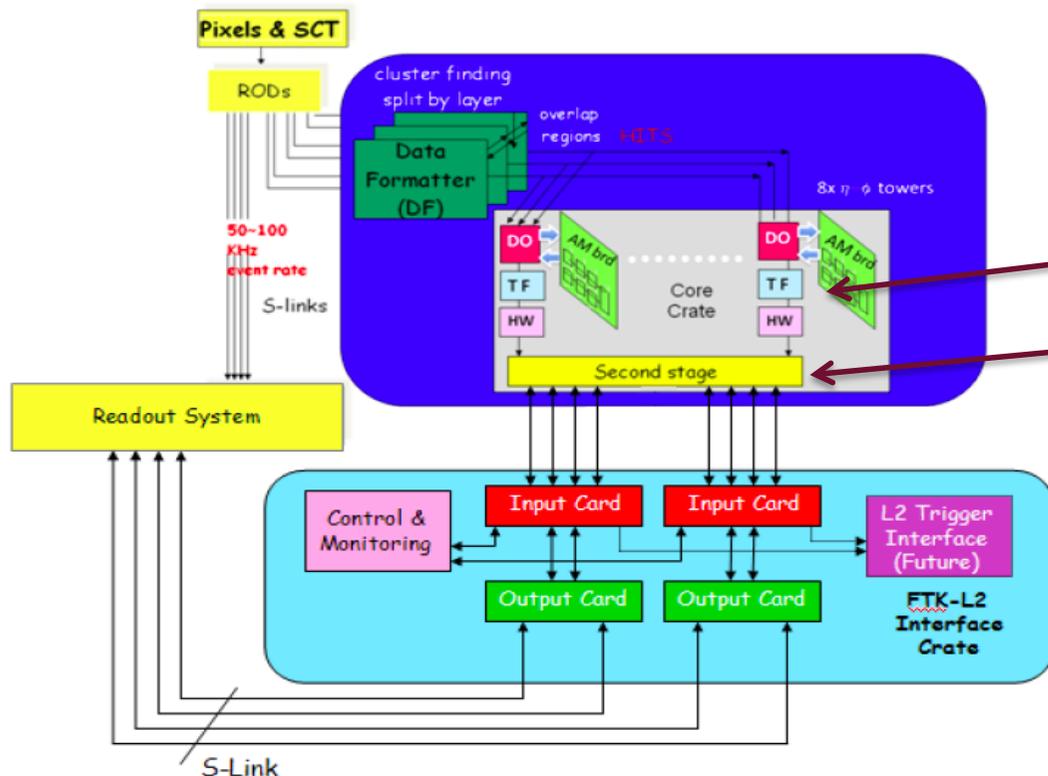
~1 ns per track

# System Overview

Core crates with processing units (pattern matching, track fitting)  
 Data input (DF) and data output (FLIC) in separated ATCA crates



- Each core crate with 1/8 azimuthal coverage
- 4X2  $\eta$ - $\phi$  towers in each core crate, each tower with two processing units
- Overlaps to maintain high efficiency



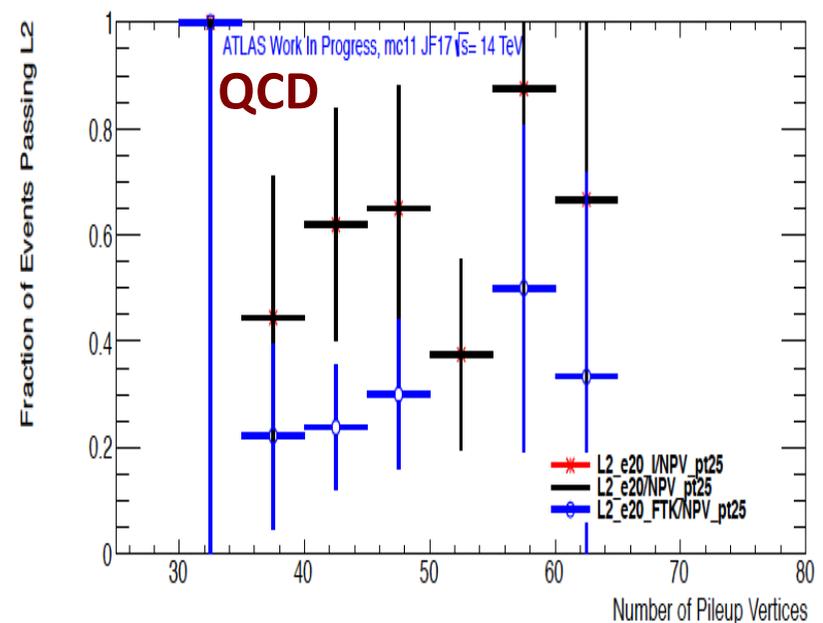
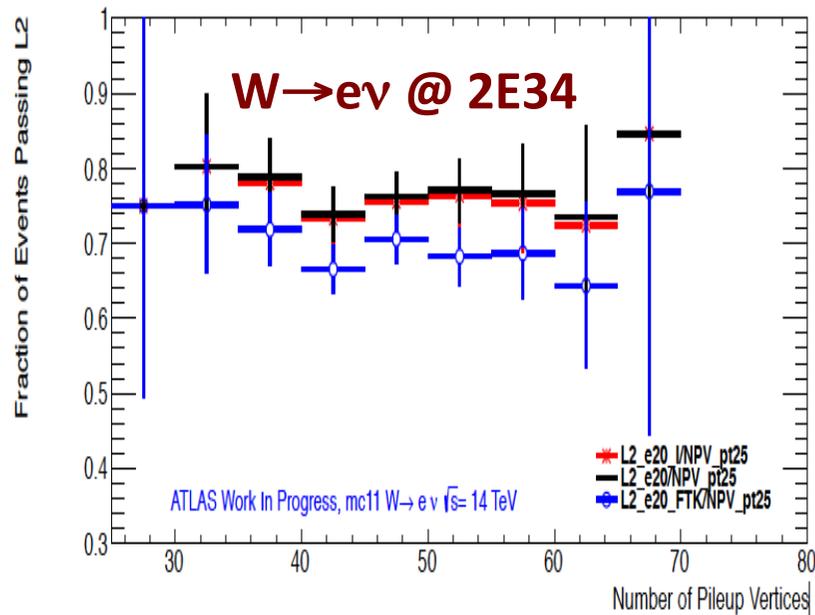
## Two stage architecture

- PIX 3 (&IBL)+SCT 4 axial, 2<sup>nd</sup> stereo
- SCT stereo layer extrapolation & 11-layer fit



# Electron Isolation

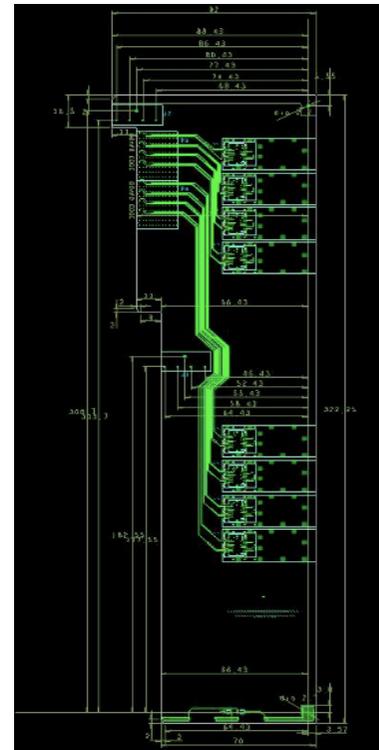
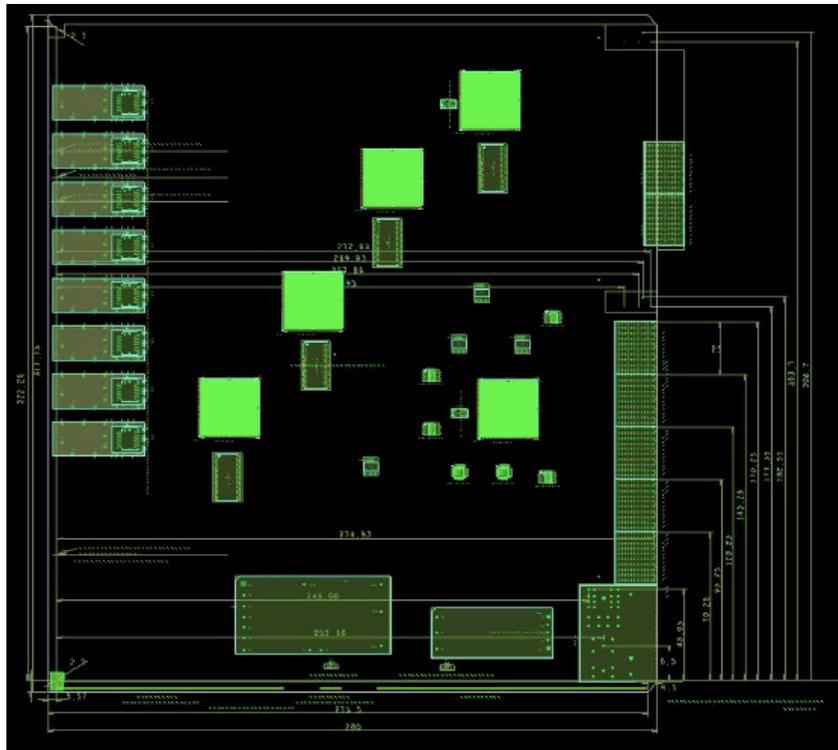
- Electron isolation in LVL2 inherited from the Level-1 calorimeter trigger
- Calorimeter based electron isolation may degrade with high pileups at high luminosity
- Offline-like tracks of the full event available at the beginning of LVL2 from FTK
- The effectiveness of track isolation on top of current LVL2 being investigated (electron efficiency vs background rejection)



# FTK-LVL2 Interface Crate (FLIC)

- ATCA technology; one shelf with full mesh backplane
- Input card receiving data from core crates
- RTM sending data to ROSs
- Processor blade for control & monitoring

Board layout almost finished and testbed ready



# FLIC Prospective

- Large bandwidth margin and also suitable for future higher performance
- Capability to merge data streams per event via fabric
- Processor blade to perform trigger functionalities such as beam spot, Z of vertices ...

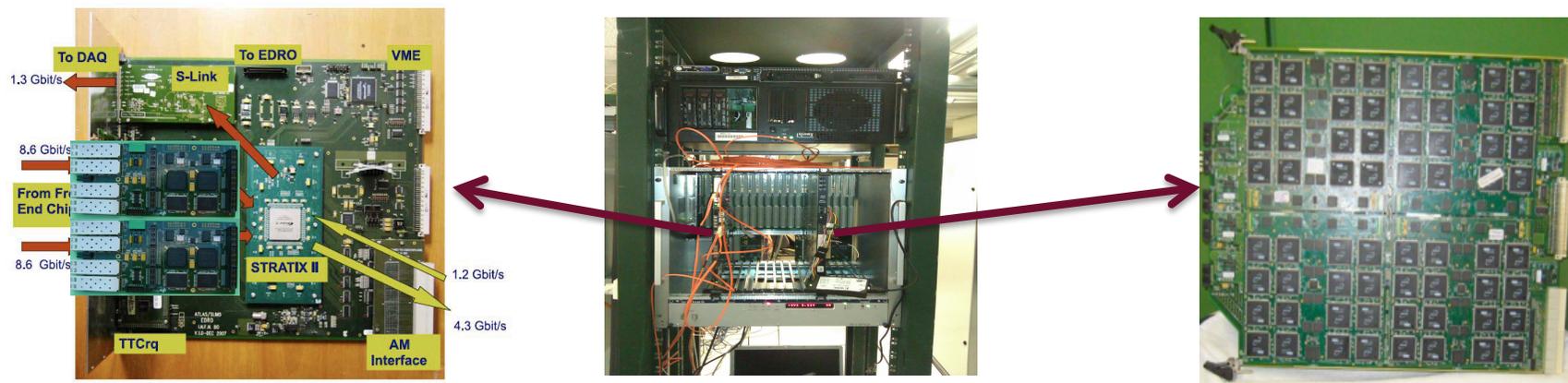
## Data Rates @ $\mathcal{L} = 3E34$

- 100 KHz max. trigger rate
- $\sim 300$  tracks/event
- 11 hits/track
- $\sim 100$  bytes/track + 40/event
- ⇒  $\sim 3$  GByte/Sec input rate
- ⇒  $\sim 3$  Gbps per Core Crate



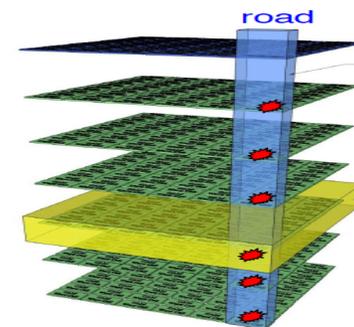
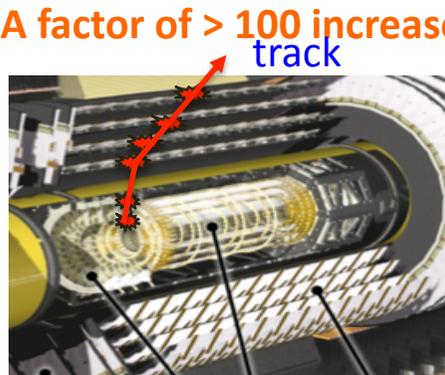
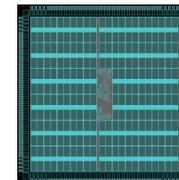
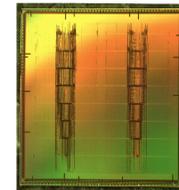
# FTK Vertical Slice

- **Objective**
  - Integration of prototype components with ATLAS TDAQ
  - Verifying hardware under normal data taking conditions
  - Exercising FTK data readout with other detectors during collision data taking
- **Work in Progress**
  - **Duo-output HOLA cards installed and tested**
    - Fibers routed and ready to connect
    - Primary channel working correctly as the regular card
  - Primary hardware, firmware and software being tested in the lab
    - FTK specific components and ATLAS TDAQ standard components
    - Developing and debugging
  - **Moving to point 1 in September**



# AM Chip R&D for HL-LHC

- FTK being designed for up to Phase-I luminosity, and with current Inner detector
- Higher luminosity, new Inner detector, (Level-1 track trigger) in Phase-II
- Larger pattern capacity and faster speed demanded for AM chip subsequently
  - AM chip being used for the vertical slice
    - 180 nm, standard cell, 1X1 cm<sup>2</sup>, ~3.7K patterns/chip for 8-layer
  - AM chip being designed for FTK
    - 65 nm technology providing a factor 8 → 30K patterns/chip
    - Full custom cell providing at least a factor 2 → 60K patterns/chip
    - 1.2 x 1.2 cm<sup>2</sup> size → ~80K patterns/chip
  - 3D AM chip R&D (VIPRAM project by ANL, Fermilab & UChicago)



# Summary

- **Good progress on FTK**
- **Milestones to TDR (ANL group actively working on)**
  - **Specification documents for boards: Spring, 2011**
  - **Complete critical studies: Summer, 2011**
  - **Dual-output HOLA production start: Summer, 2011**
  - **AM chip submission: Autumn, 2011**
  - **Vertical slice moves to CERN: Autumn, 2011**
  - **Operate vertical slice with beam: Autumn, 2012**
  - **Tested prototype boards: Autumn, 2012**
  - **Complete TDR: Spring, 2013**
- **Installation in 2015 with large detector coverage**

