

PSEC Glass Tile Readout System

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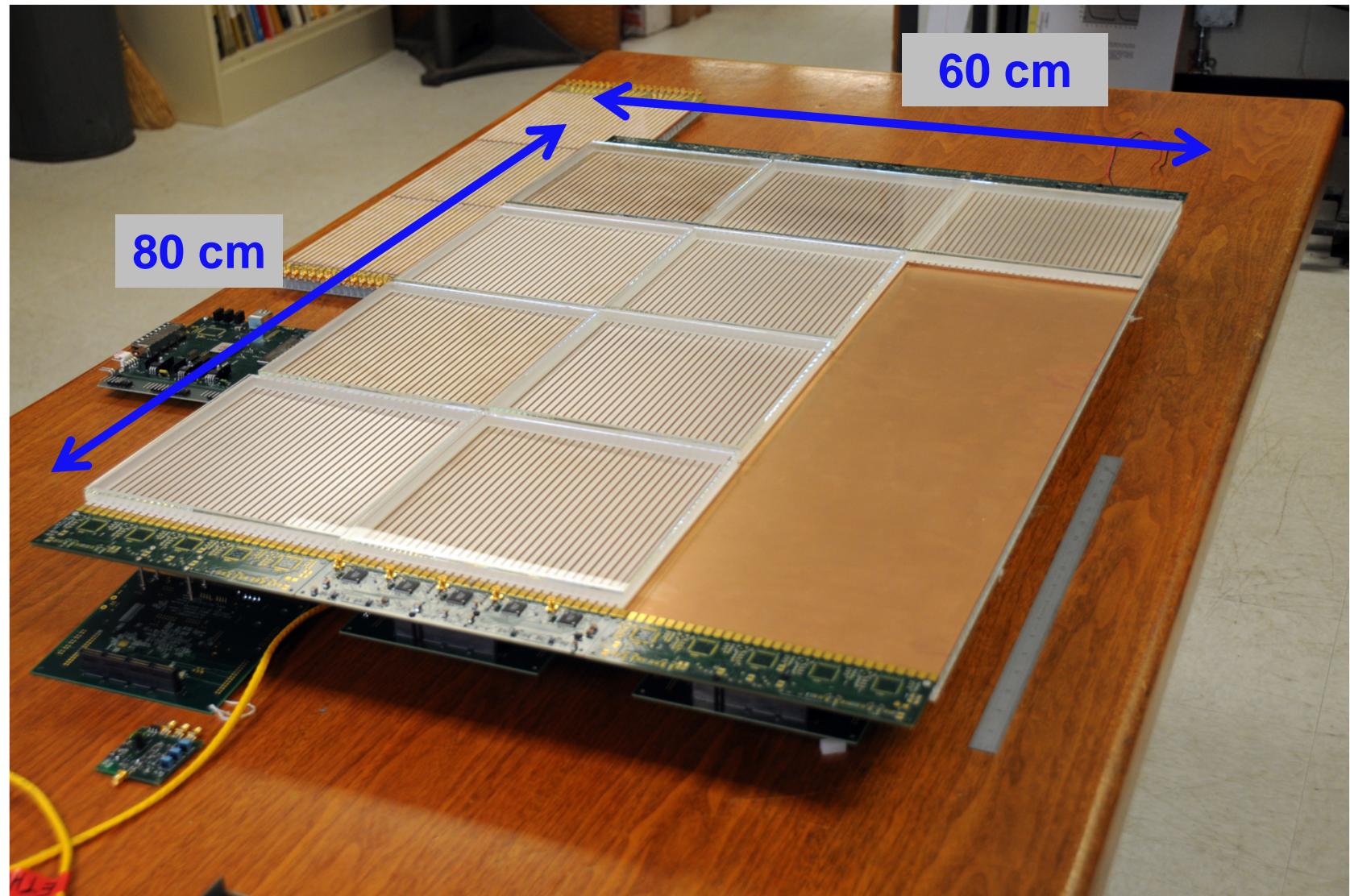
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Argonne National Laboratory

LAPPD Electronics and Integration Godparent Review
July 9, 2012

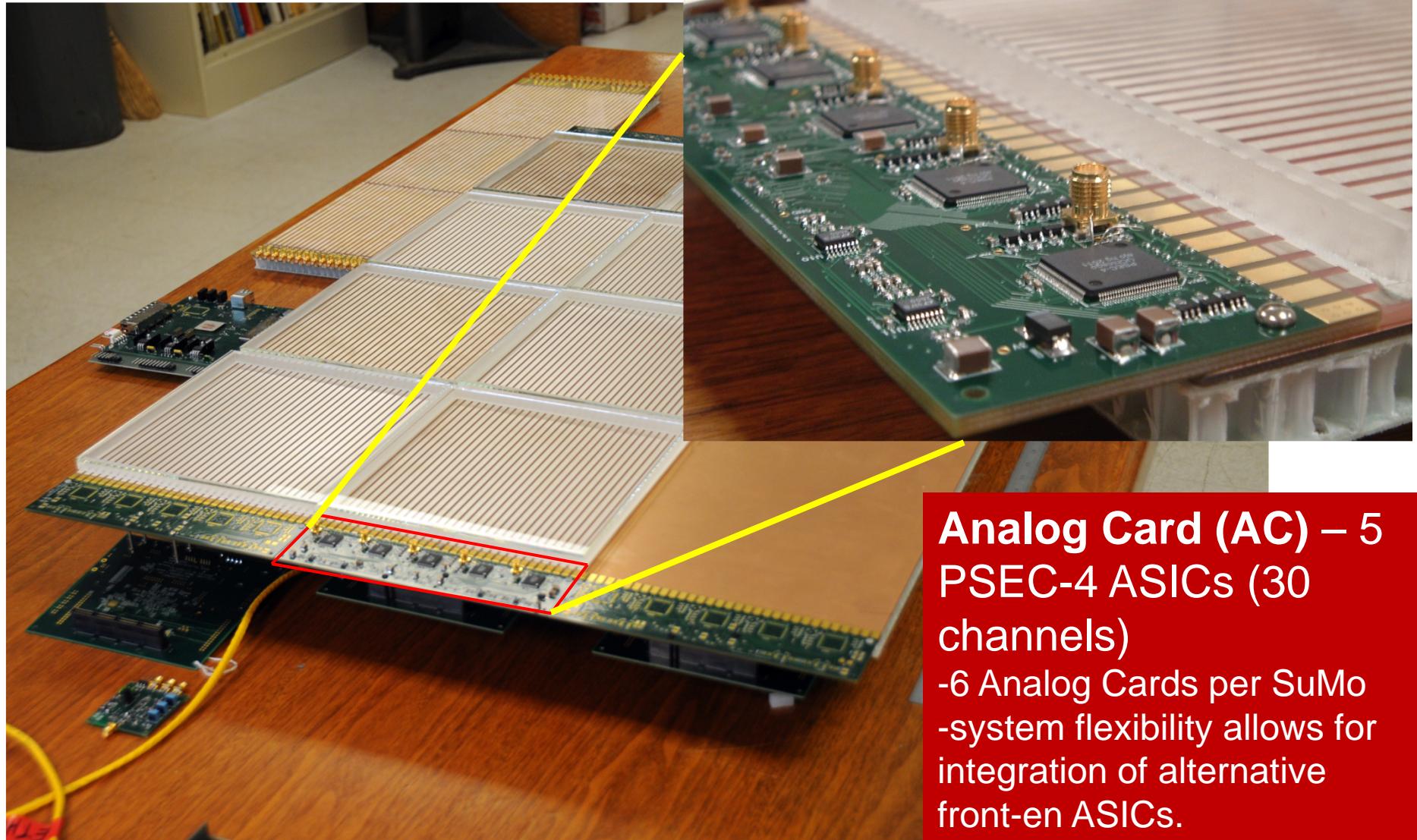
Super Module: 0.5 m^2 of photosensitive area



From Eric

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Super Module Front End



From Eric

Analog Card (AC) – 5 PSEC-4 ASICs (30 channels)
-6 Analog Cards per SuMo
-system flexibility allows for integration of alternative front-en ASICs.

The PSEC4 Waveform Sampling ASIC

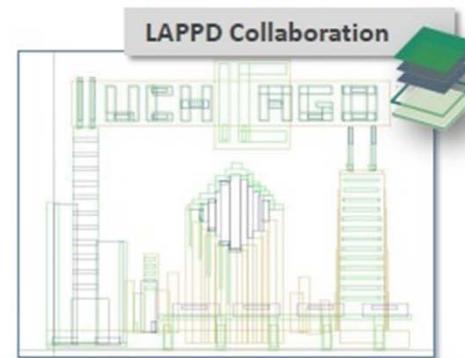
PSEC4: Eric Oberla and Herve Grabas; and friends...

PSEC-4 ASIC

Designed to sample & digitize fast pulses (MCPs):

- Sampling rate capability
 $> 10\text{GSa/s}$
- Analog bandwidth $> 1 \text{ GHz}$ (challenge!)
- Relatively short buffer size
- Medium event-rate capability (up to 100 KHz)

→ 130 nm CMOS



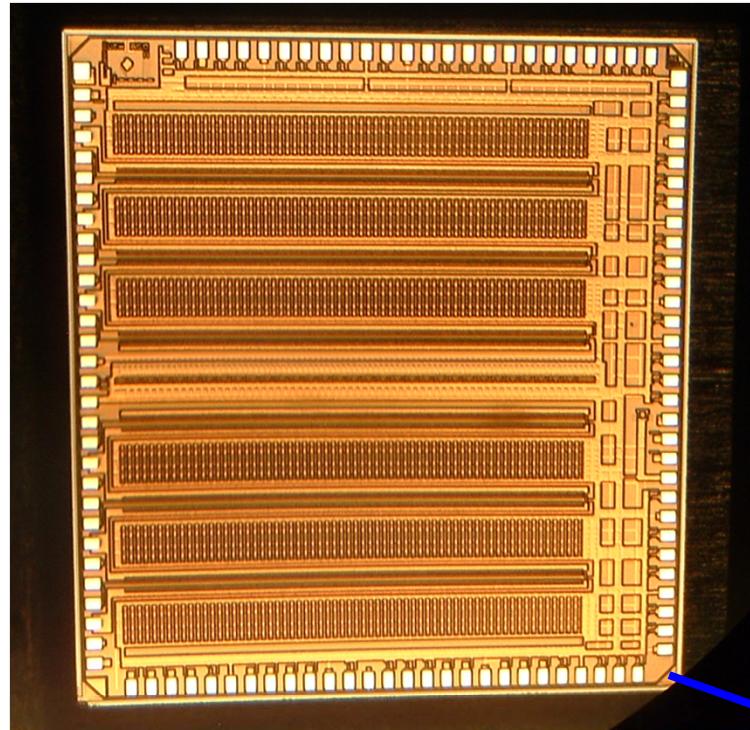
	SPECIFICATION
Sampling Rate	2.5-15 GSa/s
# Channels	6 (or 2)
Sampling Depth	256 (or 768) points
Sampling Window	Depth*(Sampling Rate) ⁻¹
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz
ADC conversion	Up to 12 bit @ 2GHz
Dynamic Range	0.1-1.1 V
Latency	2 μs (min) – 16 μs (max)
Internal Trigger	yes

10/11/2011

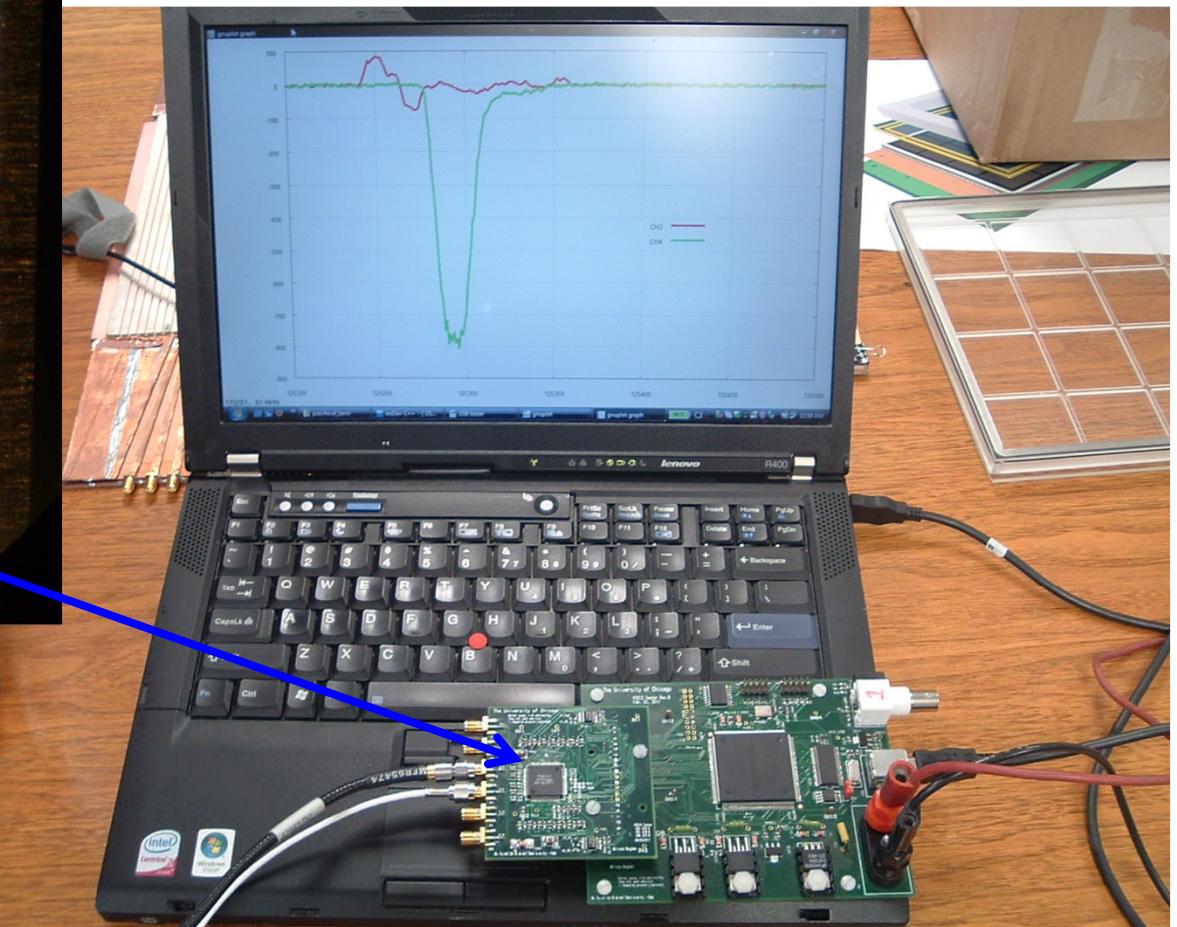
ANT'11 LAPPD electronics

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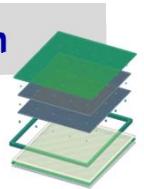
PSEC-4 ASIC



- 6-channel “**oscilloscope on a chip**” (1.6 GHz, 10-15 GS/s)
- Evaluation board uses USB 2.0 interface + PC data acquisition software



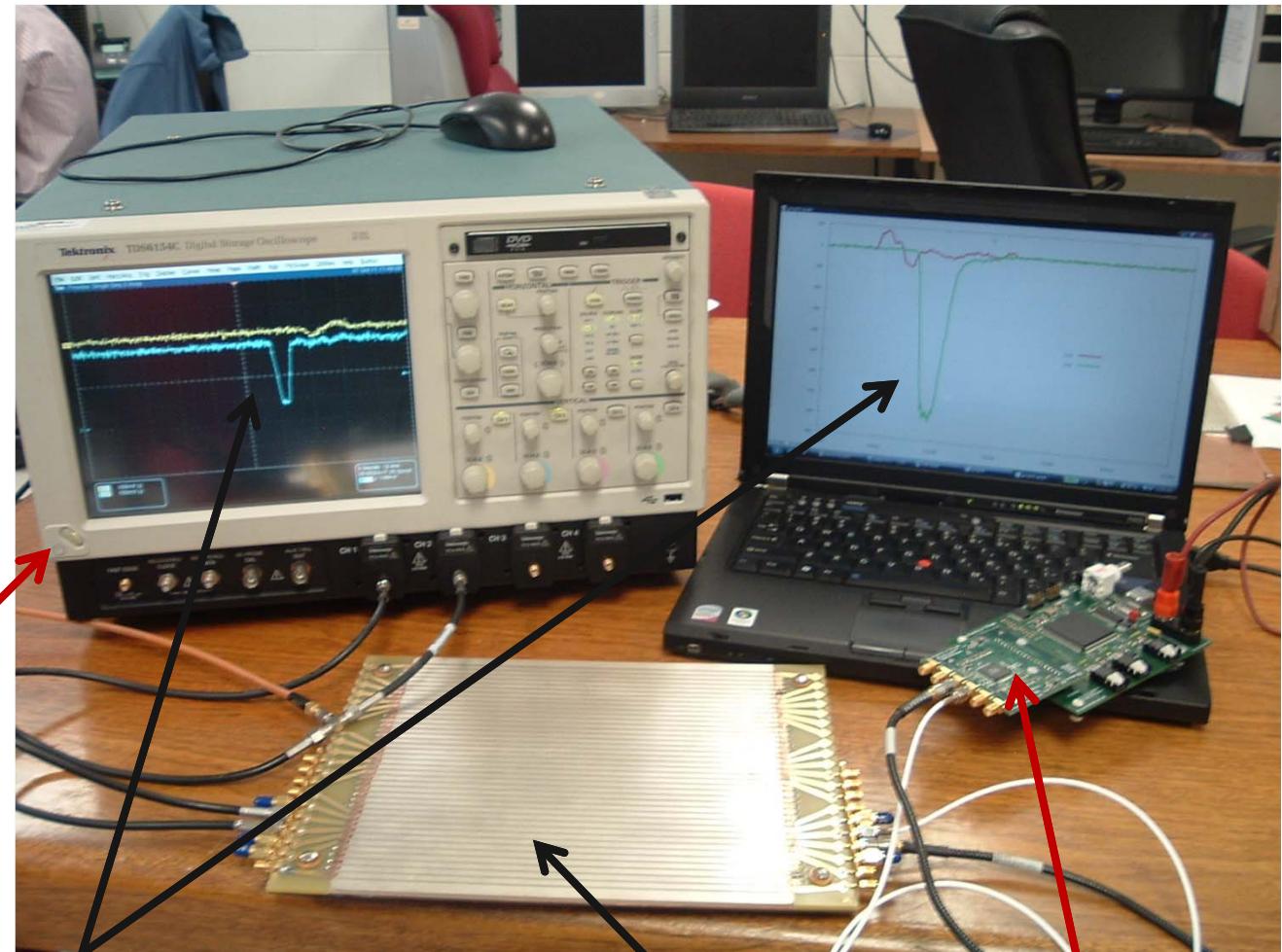
LAPPD Collaboration



Eric Oberla, ANT11

6-channel `Scope-on-a-chip'

Designed by Eric Oberla (UC grad student) working in EDG with EDG tools and engineers (H. Grabas, J.F. Genat)



20 GS/scope
4-channels (142K\$)
7/5/2012

SLAC June 2012

17 GS/PSEC-4 chip
6-channels (\$130 ?!)

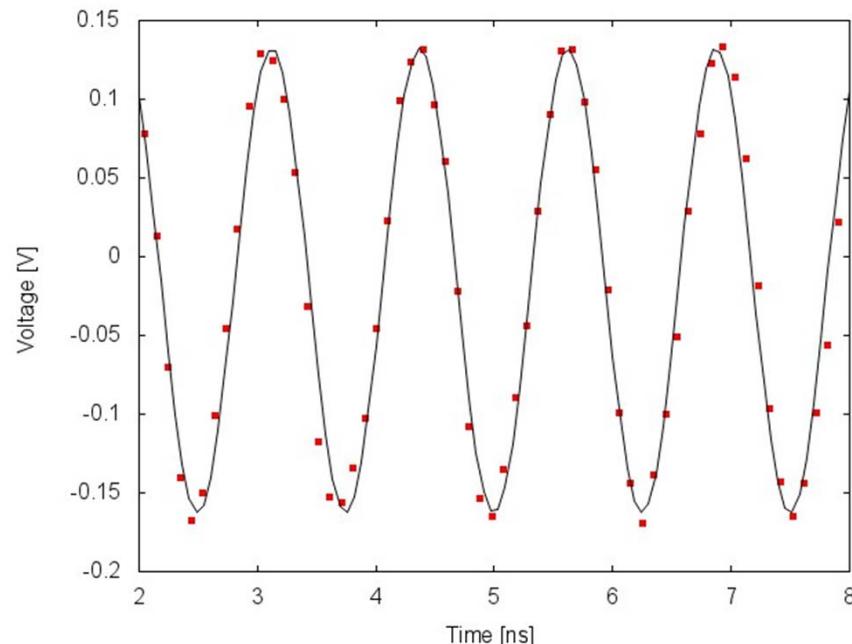
PSEC-4 Performance

Eric Oberla, ANT11

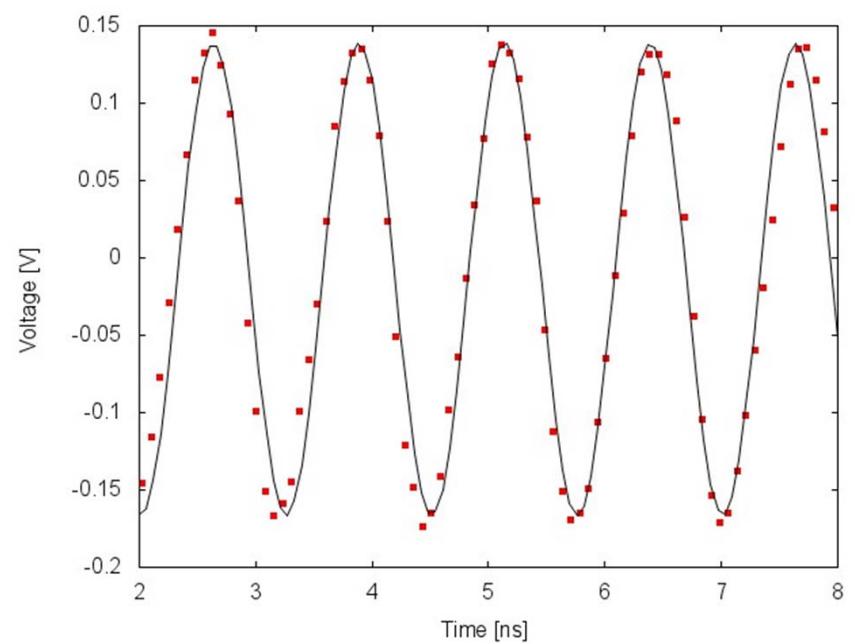
Digitized Waveforms

Input: 800MHz, 300 mV_{pp} sine

Sampling rate : 10 GSa/s



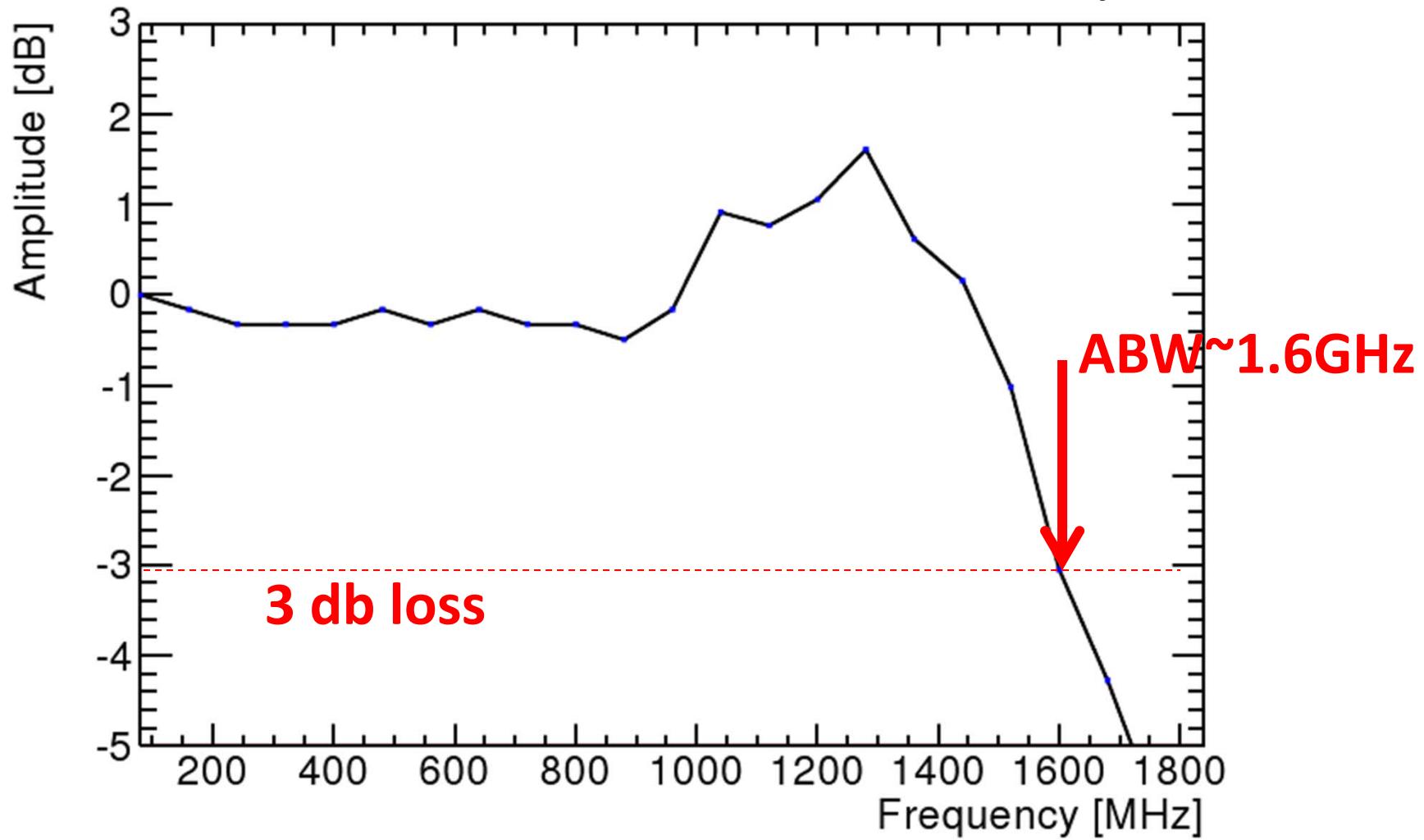
Sampling rate : 13.3 GSa/s



- Only simple pedestal correction to data
- As the sampling rate-to-input frequency ratio decreases, the need for time-base calibration becomes more apparent (depending on necessary timing resolution)

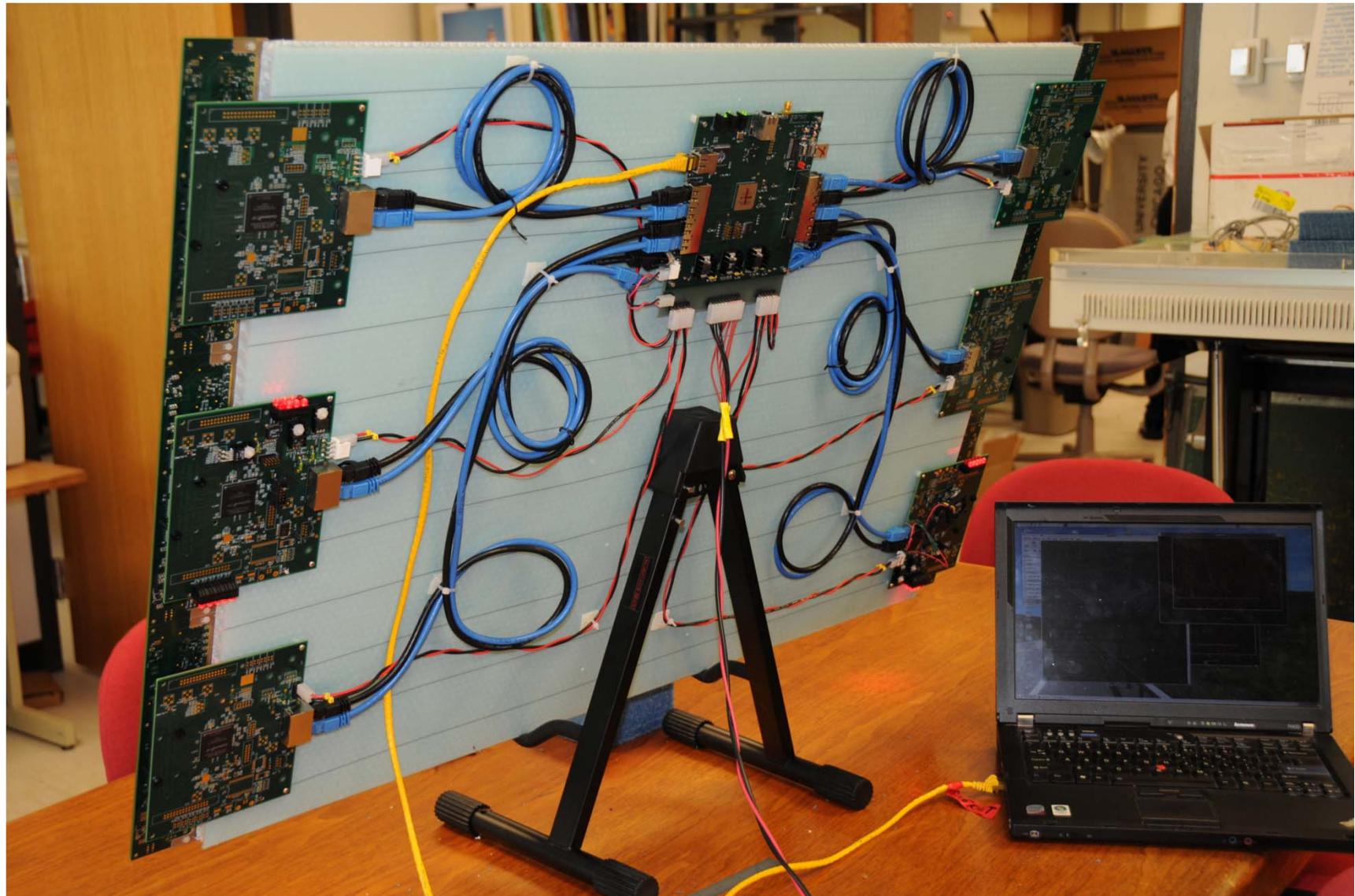
Digitization Analog Bandwidth

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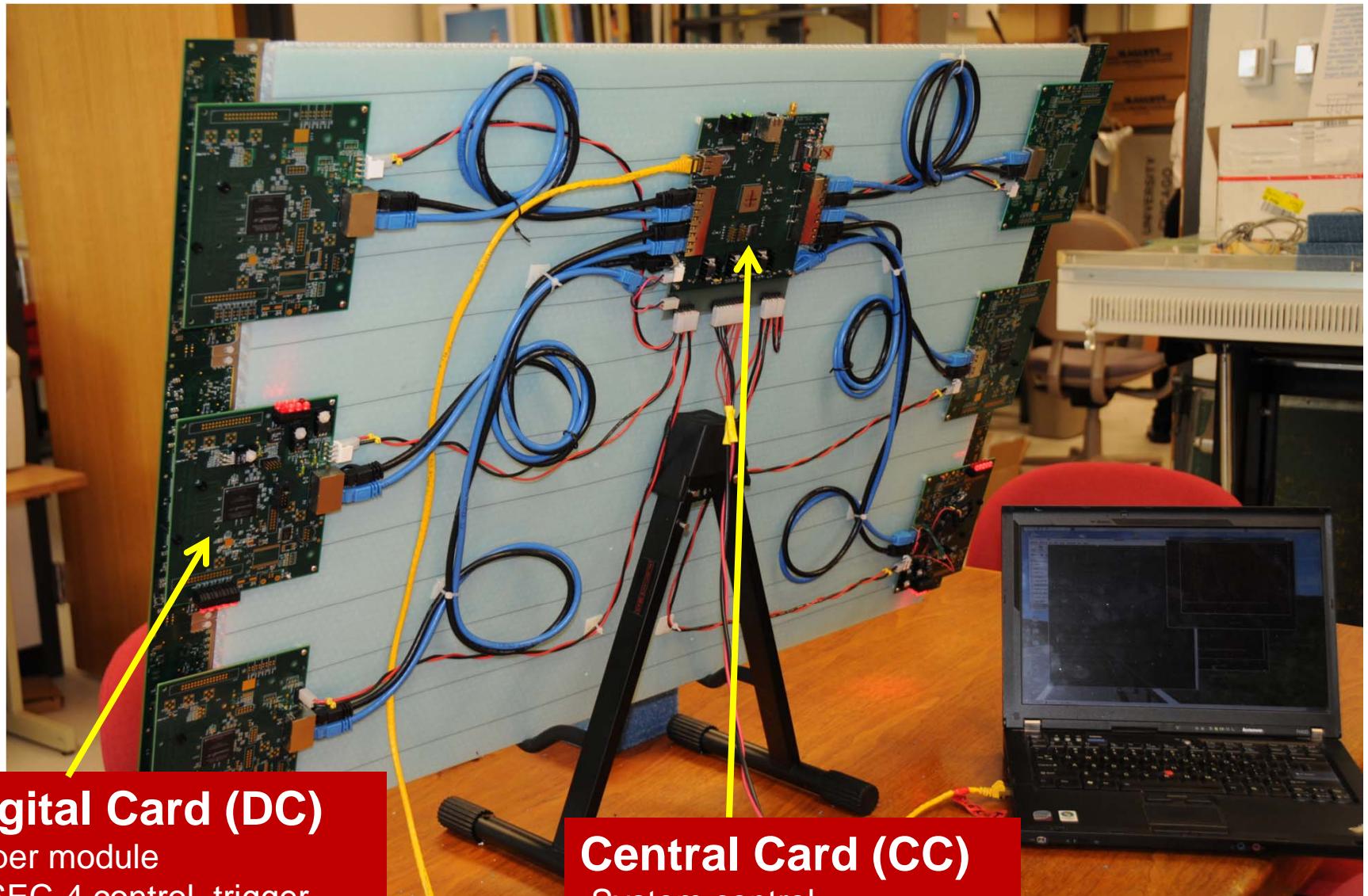
PSEC4: Eric Oberla and Herve Grabas+ friends...

Super Module: backside-integrated electronics



From Eric

Super Module: the hardware



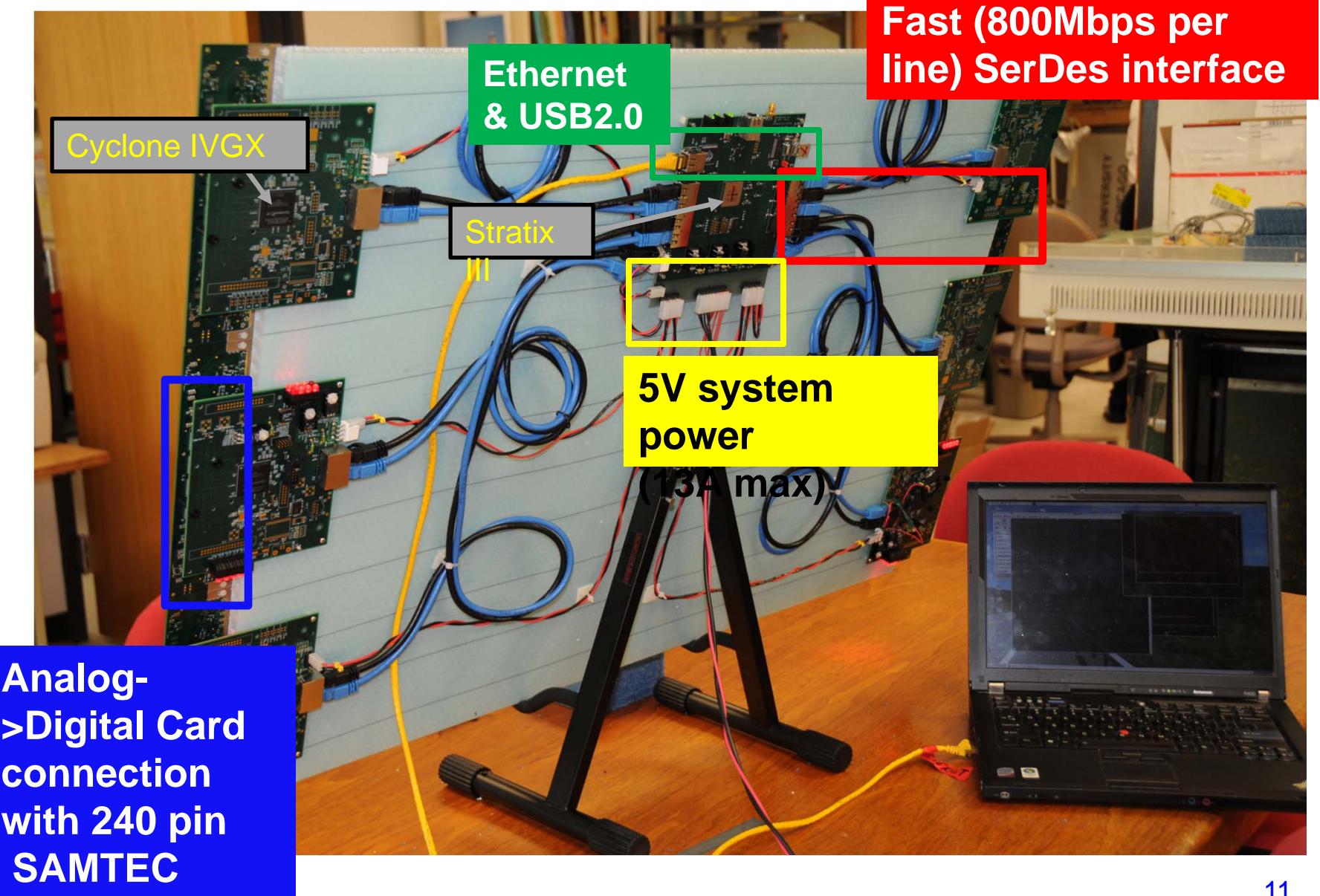
Digital Card (DC)

- 6 per module
- PSEC-4 control, trigger handling, local data reduction & calibration

Central Card (CC)

- System control
- Feature extraction
- Interface (Triple Speed Ethernet & USB 2.0)

Super Module: features



PSEC4 Readout Hardware Status

Basic Super Module Structure: 6 x Analog Cards + 6 x Digital Cards + 1 x Central Card.

Analog Card(AC):

- Rev. A board functional;
- Enough boards for the number of PSEC4 chips;

Digital Card(DC):

- Rev. A works with minor bugs (USB connection not functional yet):
 - use LVDS ;
 - fix is in the works with little mezzanine card;

Center Card(CC):

- Rev. A board designed to service 4 DCs;
- Will need Rev. B board to service 6 DCs for a full Super Module.

Readout Firmware/Software Status

Communication:

- AC to DC: functional;
- DC to CC (320MBPS LVDS): Firmware almost finished - under testing now;
- CC to CPU:
 - USB Firmware/Software exists - under testing now;
 - Ethernet Firmware design not started yet;

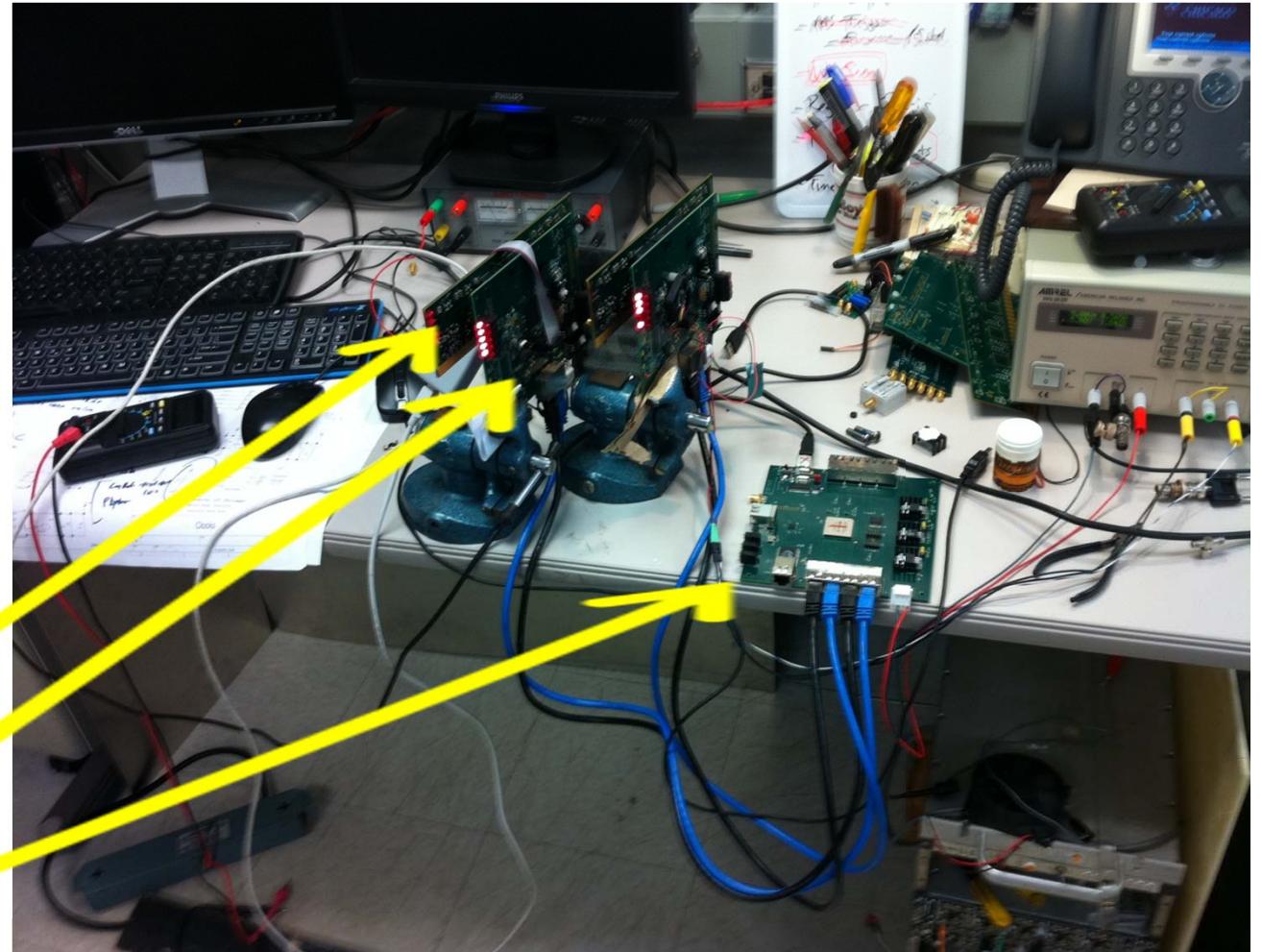
Trigger:

- Local Self Trigger (AC/DC) designed/tested on the PSEC4 Evaluation Board;

Data Processing:

- Various Data Reduction Firmware Designs were implemented and simulated;

Testing Status



Electronics for 1-tile row:

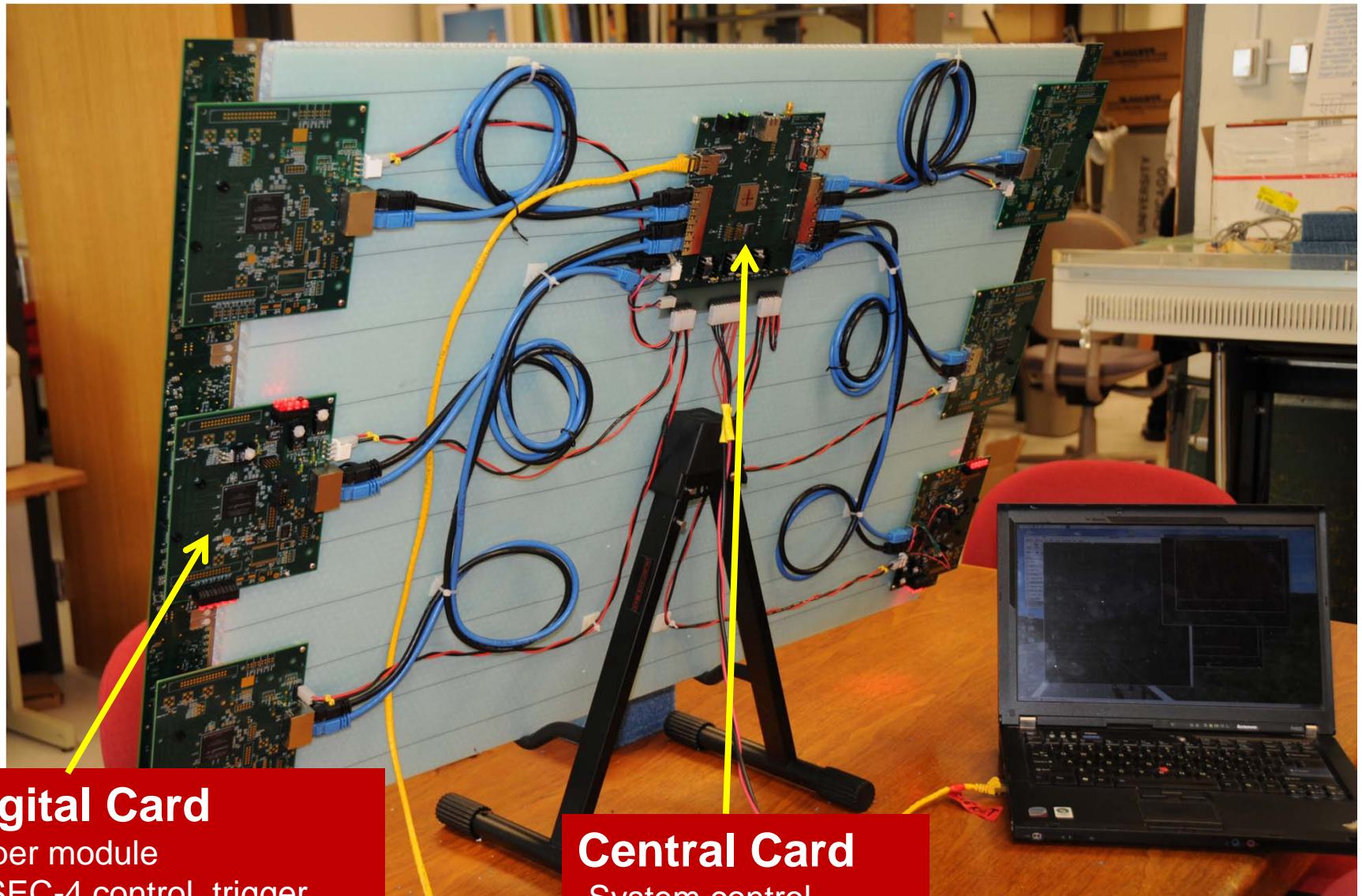
- 2 Analog Cards
- 2 Digital Cards
- 1 Central Card

In preparation for the vertical slice test

DAQ System Plans

- Finish and Test Basic Firmware/Software ;
- Complete DAQ for 1-tile row Super Module to be used at APS (by end of July);
- Finish and Test Firmware for: multi-event buffering, data reduction, etc.
- Finish and Test Firmware for Central Card Ethernet communication;
- Design and build Rev. B Central Card to service 6 Digital Cards (4-6 weeks);
- Build and Test DAQ for a full Super Module;
- Design and build Optional Alternate Analog Cards for different ASICs (4-8 weeks each).

Super Module: the hardware



Digital Card

- 6 per module
- PSEC-4 control, trigger handling, local data reduction & calibration

Central Card

- System control
- Feature extraction
- Interface (Triple Speed Ethernet & USB 2.0)