LAPPD Electronics

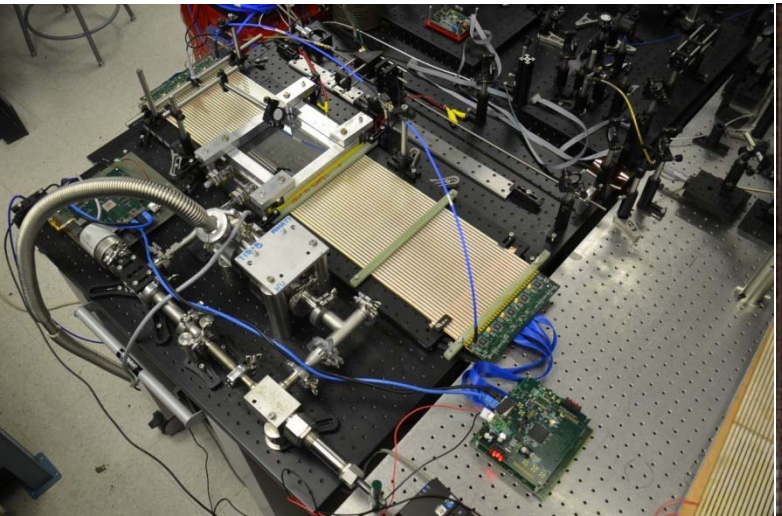
Mircea Bogdan, Henry Frisch, Craig Harabedian,
Razib Obaid, Mary Heintz, Eric Oberla
University of Chicago

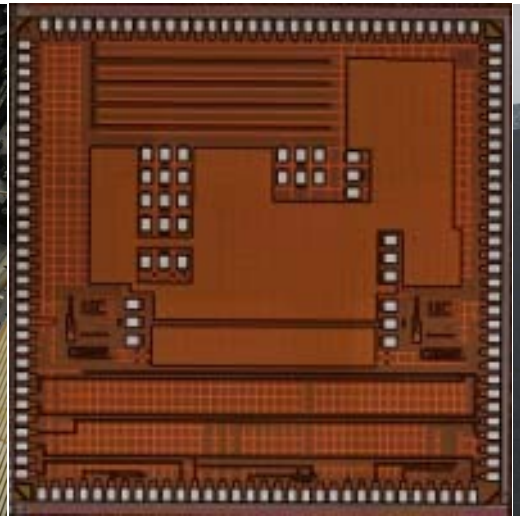
Matt Andrew, Kurtis Nishimura, Gary S. Varner
University of Hawai'i at Manoa

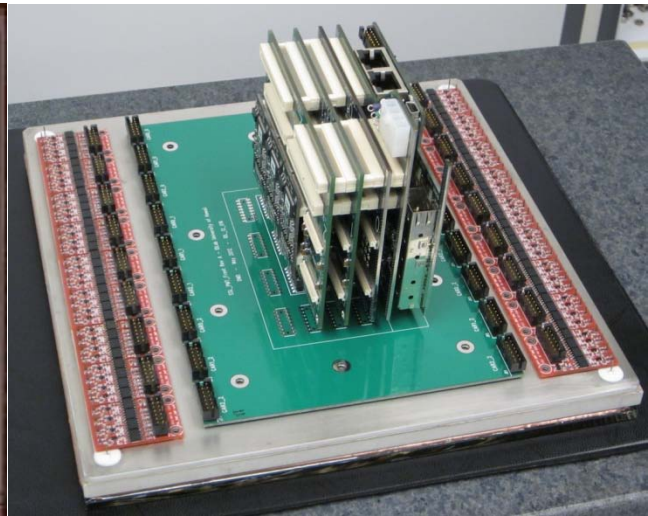
Jean-Francois Genat, Herve Grabas
Universite Pierre et Marie Curie – Paris VI, France

for the LAPPD Collaboration

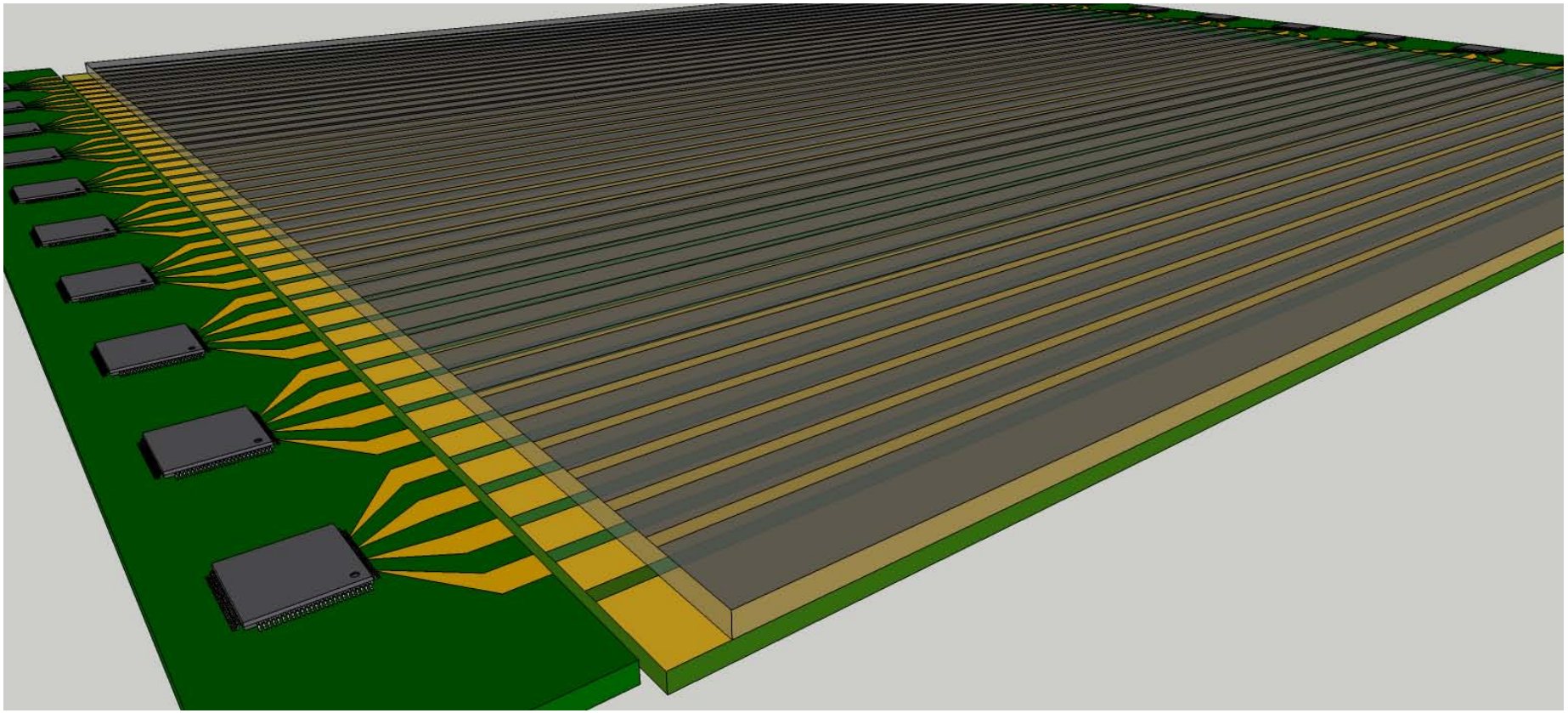
18-DEC-2012 == DOE Review at ANL







Ideal integrated electronics for a "complete" Photodetector

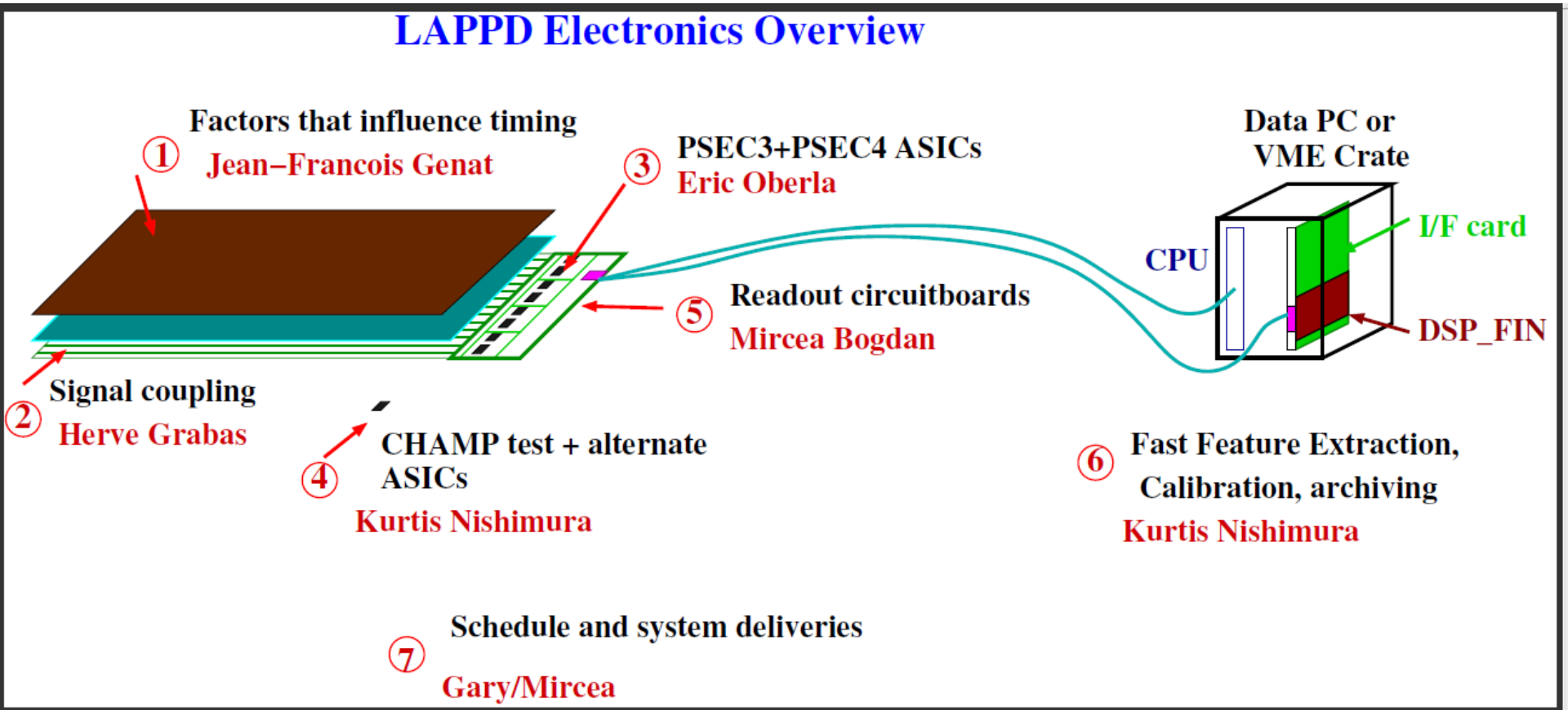


- DC power in, fiber optic out
- Integrated photon → electrons → T,Q → data out

Electronics Overview

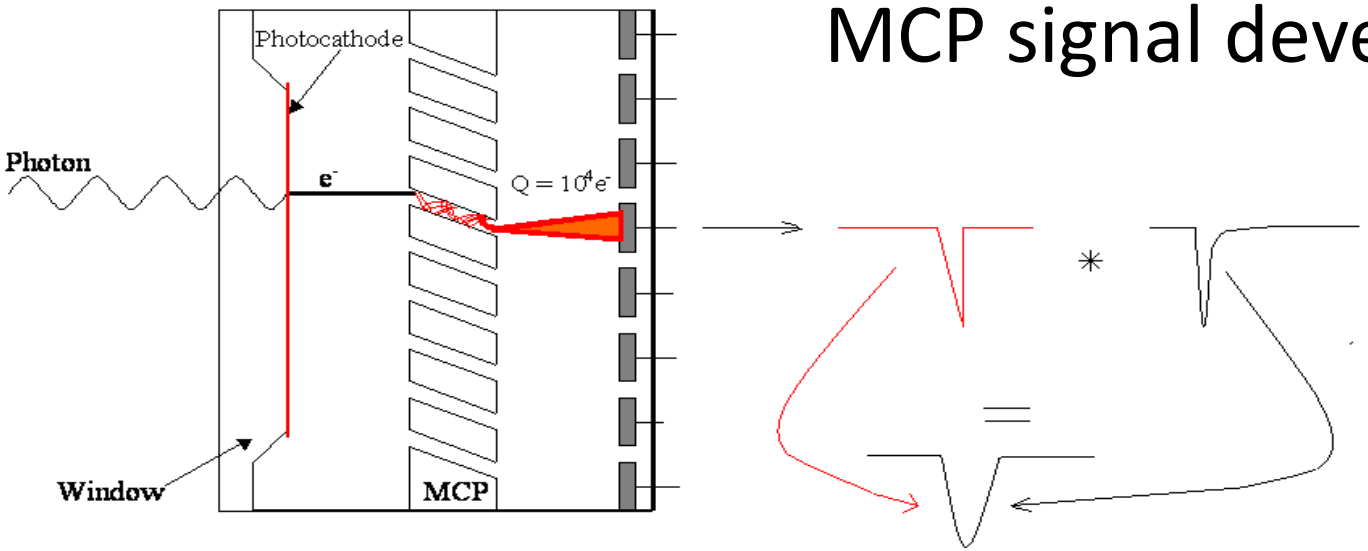
- Readout support for glass tile array and ceramic tiles
- 2 specific front-ends and common back-end infrastructure
- PSEC family ASIC for ultimate timing (spatial) resolution; portfolio of ASIC solutions (application-specific)
- Experience operating readout systems at ANL, Chicago, Hawai'i and SSL (defer performance test results until next talk)
- Support of systems for first adopters

Many Aspects to the Electronics



- Addressing all aspects needed to realize integrated PD goal
- Overview only – much fundamental work underlying

MCP signal development



MCP signal rising edge: qE = ma $tr = l\sqrt{2m/qV}$

l = 1mm, E=100V/mm, tr=250ps

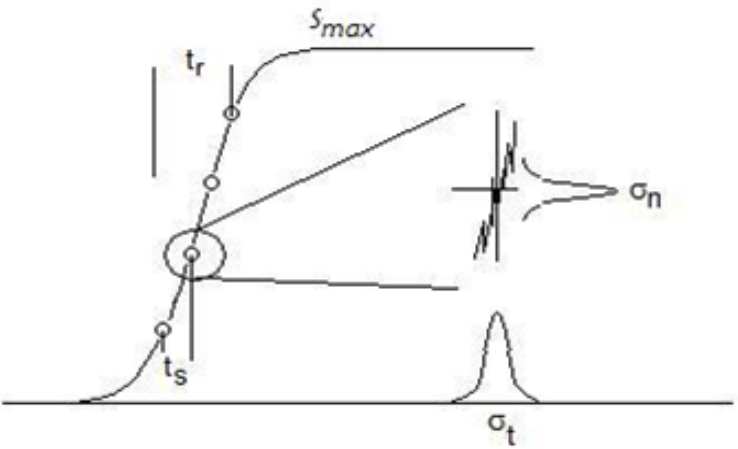
- First gap: 10ps
- Assume 2-stage pores TTS of 20ps
- Anode gap: 10ps
- Noise: 20ps

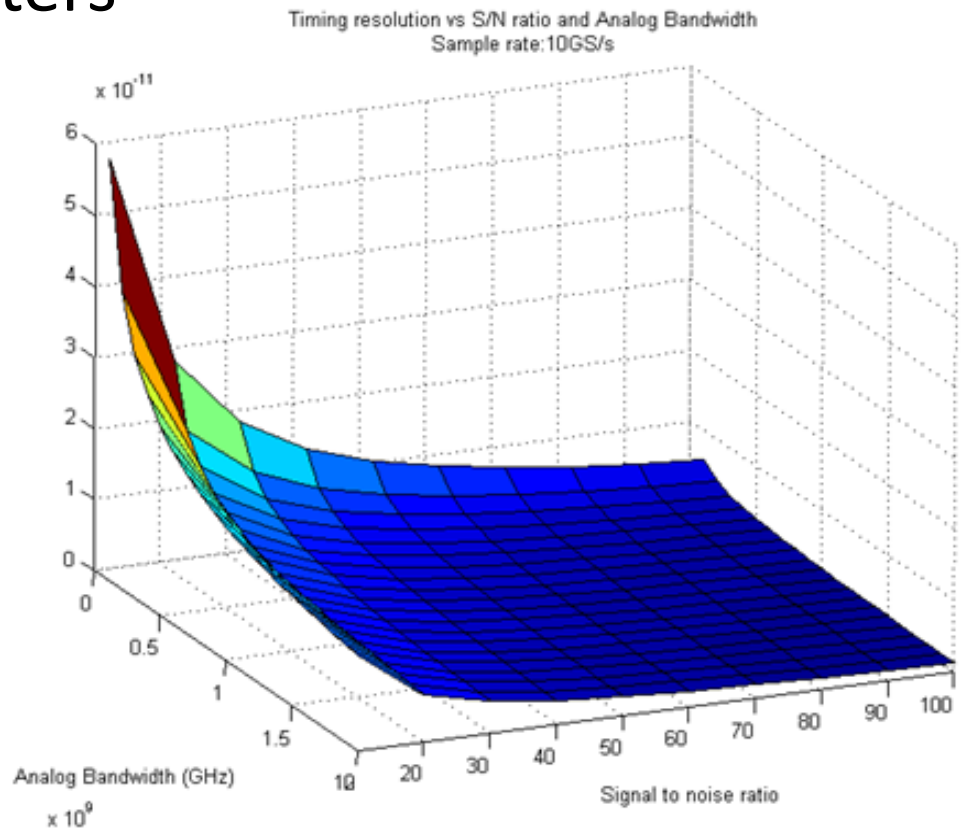
Total is 32ps

(Measured HPK SL-10 1'' x 1'' is ~35ps [core])

Understanding what matters

Transit Time
Noise$_{detector}$
Rise time
Gain (Signal/noise)





$$S = G\ Npe$$

Electronics:
Noise$_{elec}$
Sample rate
Analog bandwidth

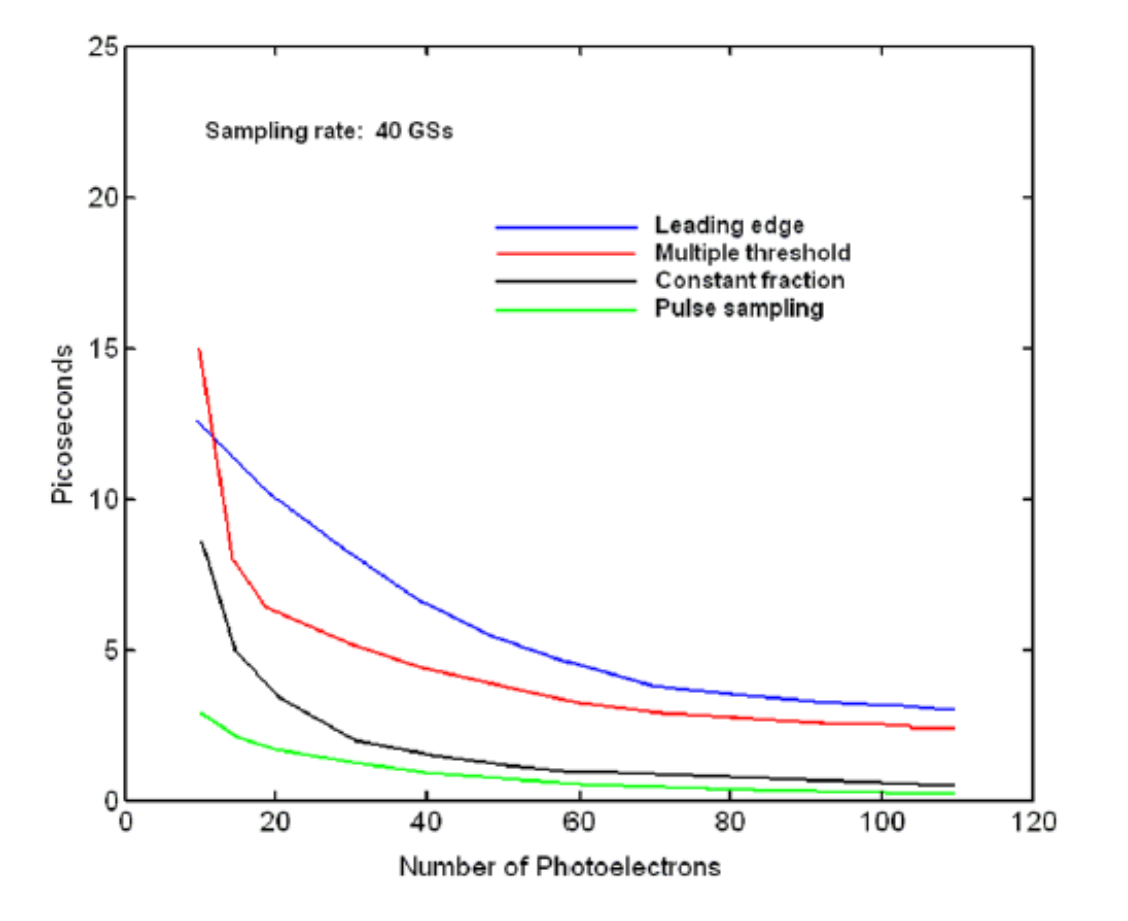
$$SN = S_{max}/\sigma_n \qquad \sigma_{t,n} = \frac{\sigma_n}{\sqrt{n}}$$

$$\sigma_{t,n} = \frac{\sqrt{t_r t_s}}{SN} = \frac{1}{SN}\sqrt{\frac{0.35 t_s}{abw}}$$

Timing Extraction Simulations

How to get to picosecond timing

- Four algorithm models compared in simulation
- In principle, **pulse sampling** gives the best timing result
- To realize this performance, sampling frequency is taken to be 2× the fastest harmonic in the signal: 10Gs/s.

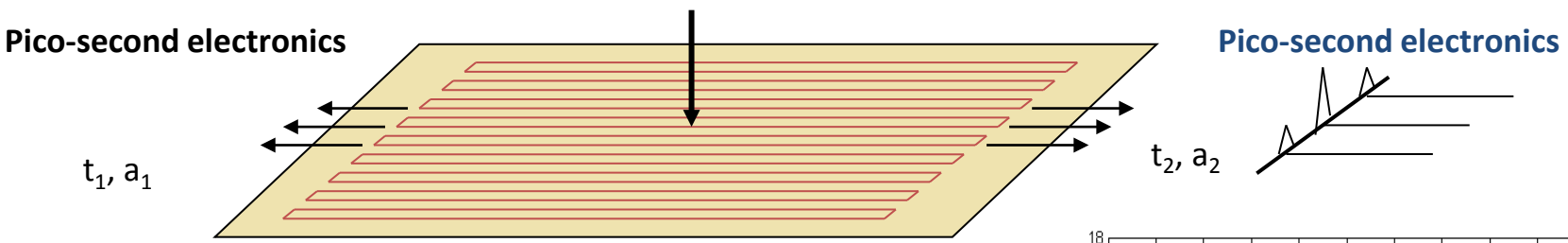


***Nucl.Instrum.Meth.A607:387-393,2009**

Picosecond timing and 2D position for large area detectors: delay lines and Waveform Sampling

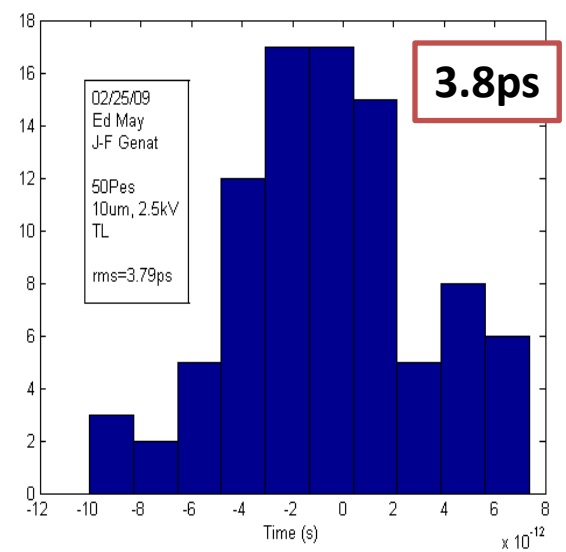
Delay line readout and pulse sampling provide fast timing (2-10ps).
→ Delay lines should have a signal bandwidth matched to the detector

Fewer electronics channels for large area sensors



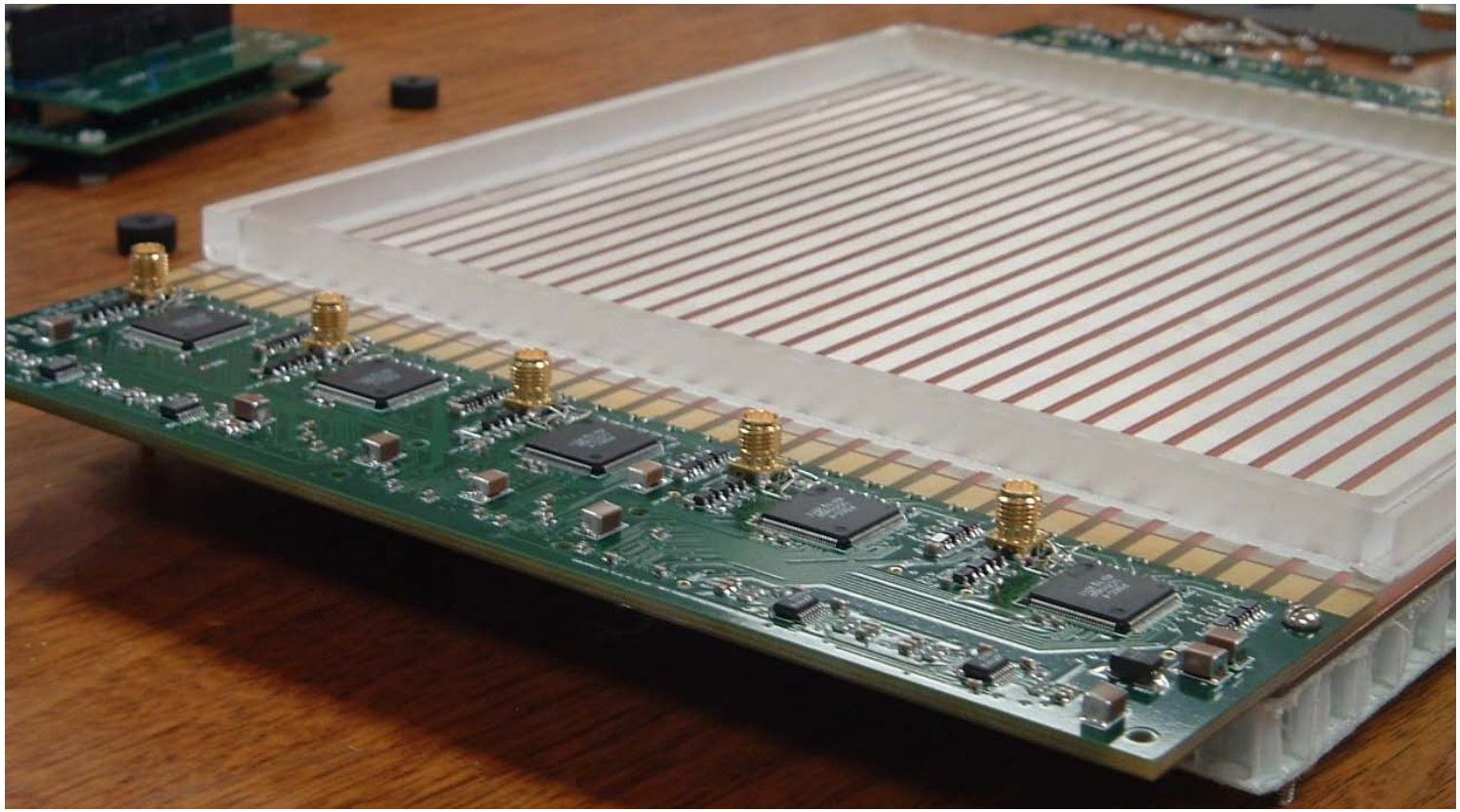
3.8 ps translates in 190 μm position resolution with 50 photo-electrons

½ (t_1+ t_2) = time
v(t_1-t_2) = longitudinal position
$\Sigma \alpha_i a_i / \Sigma \alpha_i$ = transverse position



The electronics contribution to spead is small:
3.8ps / sqrt(2) = 2.7ps,
For 50PEs, MCP is 30ps / sqrt(50) = 4.2ps, equal at 100 PEs

Understanding signal coupling

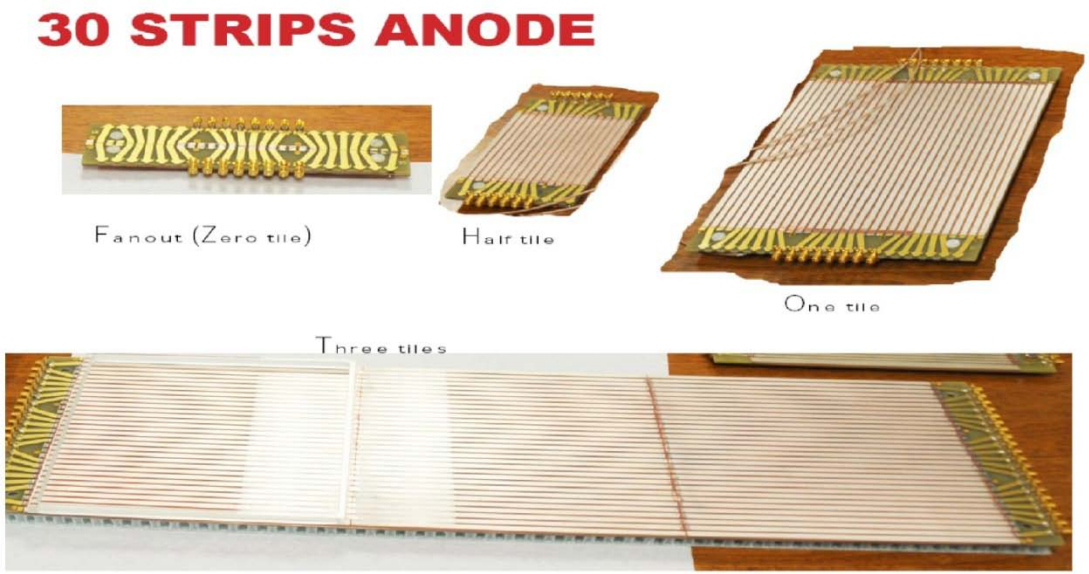


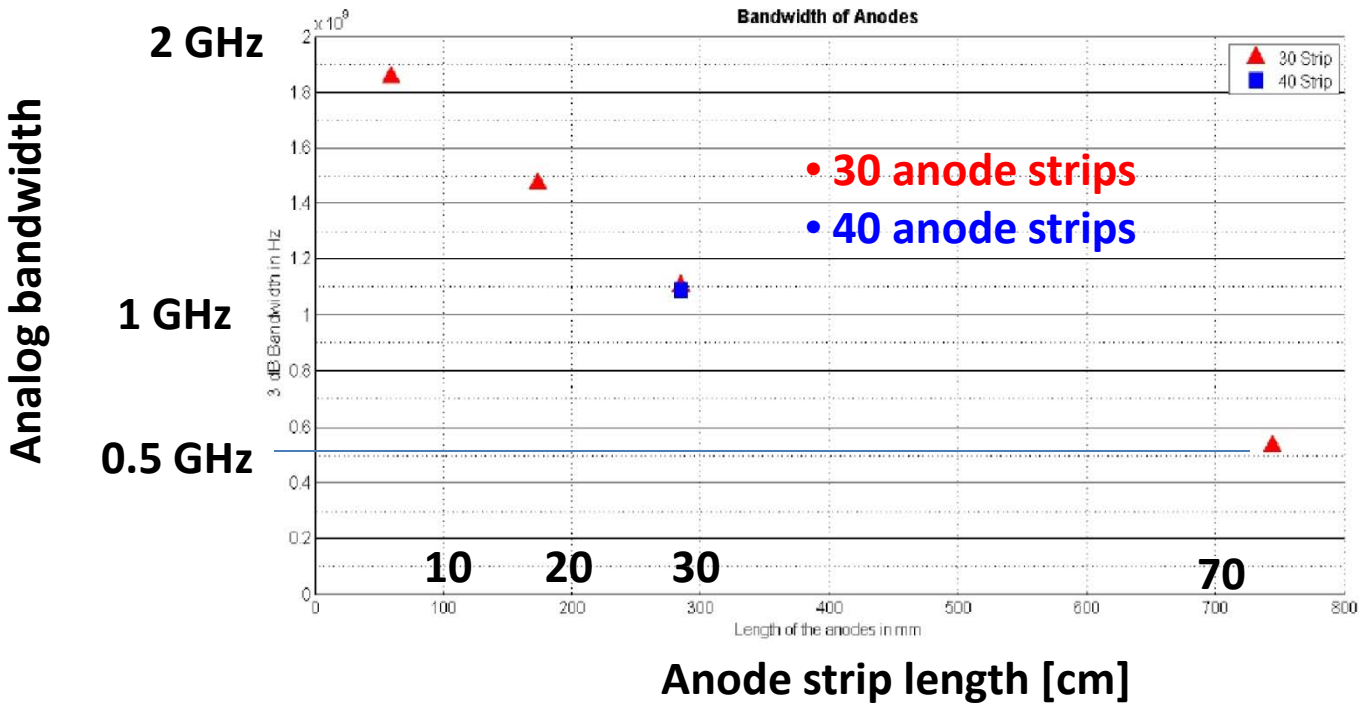
Key issues:

- Optimizing signal coupling (strip width, gaps, impedance)
- Matching analog bandwidth for signal transmission
- Coupling into the readout ASICs

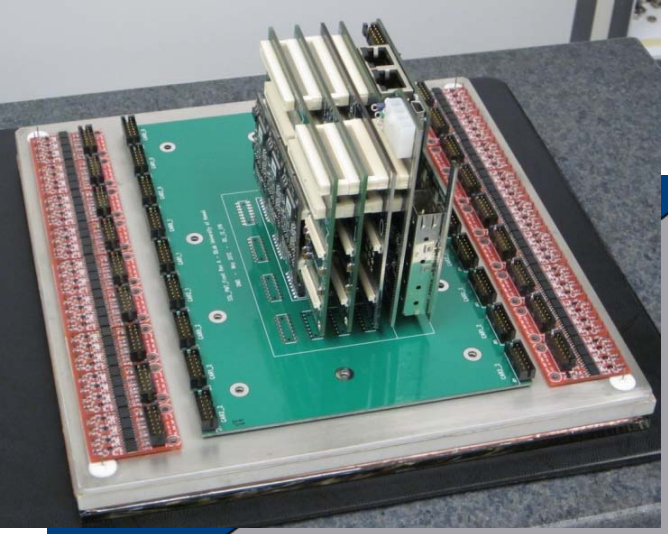
Stripline Readout

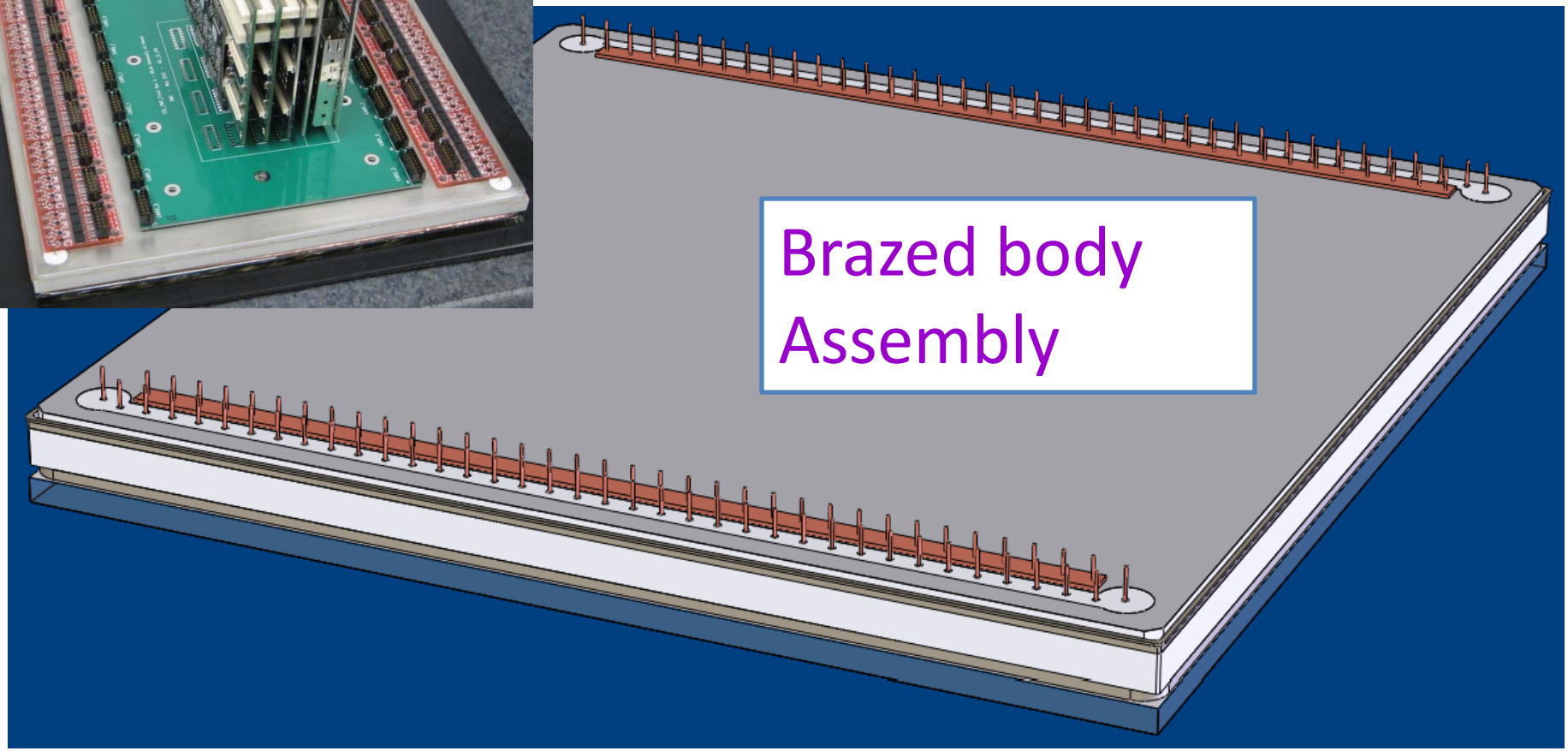
-- silkscreen on glass





Ceramic design





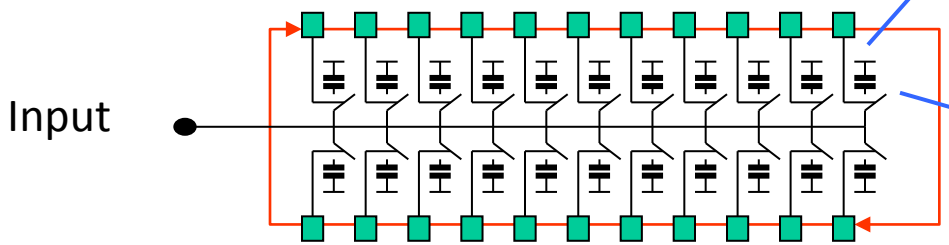
- Mechanically different configuration
- Leverage Belle II iTOP HW/FW development effort
- Single p.e. TTS limitation

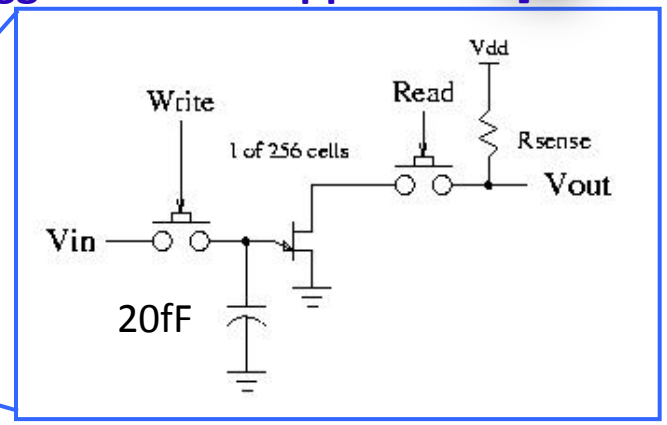
Switched capacitor array sampling: '*analog down-conversion*'

LAPPD Collaboration

[GHz sampling→ 10-100 MHz readout: useful in most 'triggered event' applications]

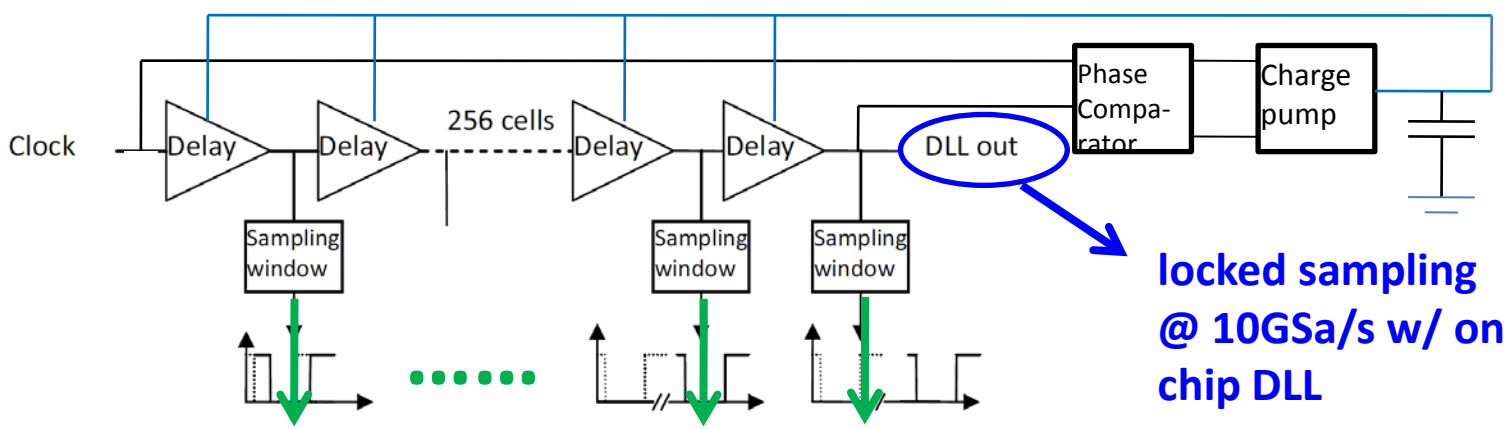
Write pointer passed along array - generates 'sampling window' (~5-10 switches closed at once):





Tiny charge: 1mV ~ 100e$^-$

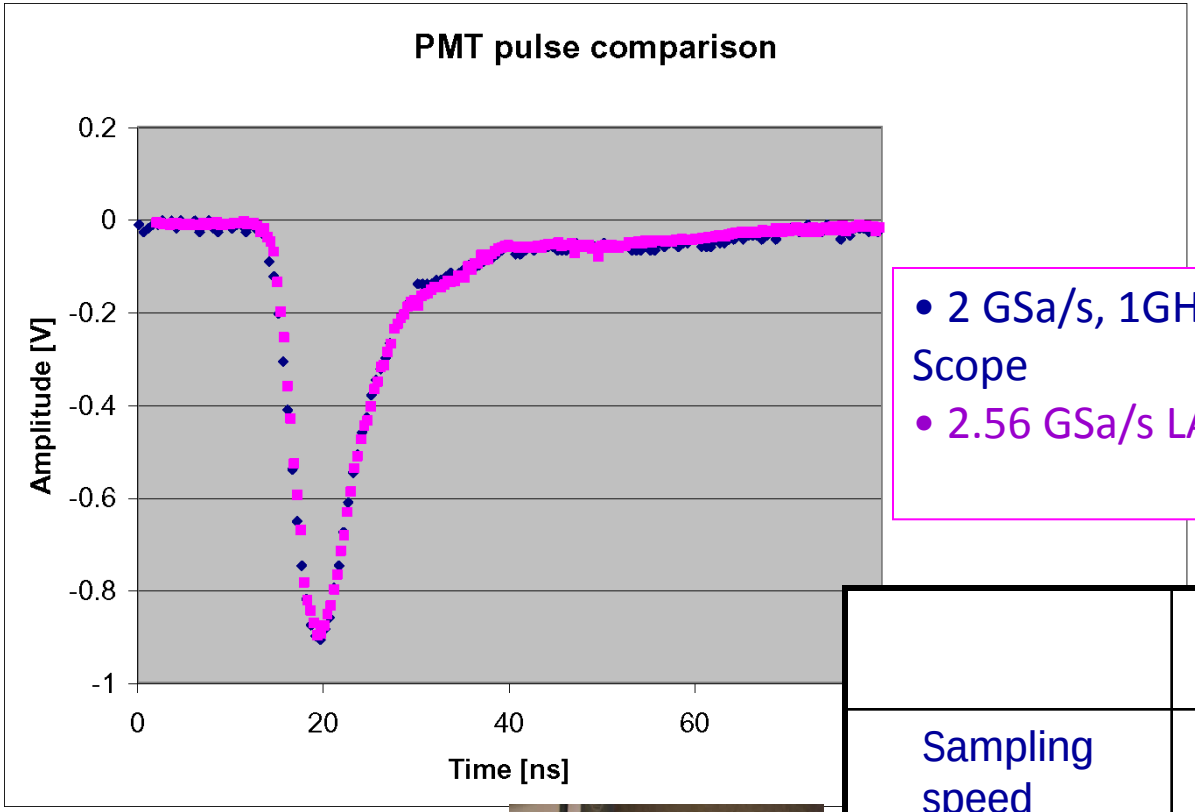
Timing generation with a delay locked loop (DLL):



locked sampling @ 10GSa/s w/ on chip DLL

To switched capacitor array – sample & hold

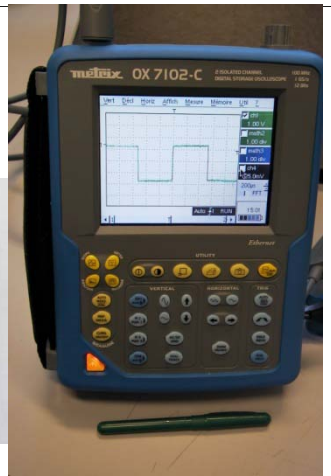
A rapidly developing technology



- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB

	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< $10 (vol)	> 100$

"oscilloscope on a chip"

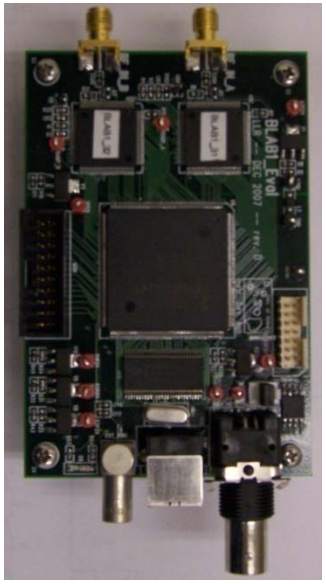


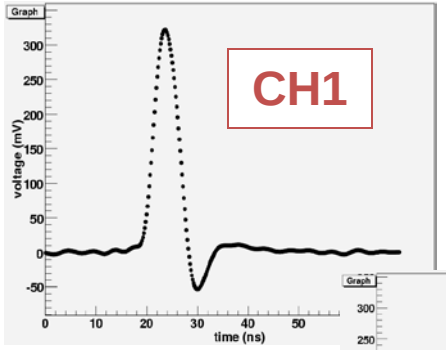
One of a number of

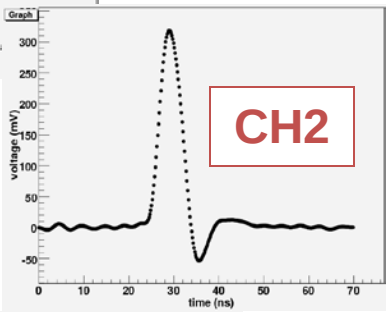
"oscilloscopes on a chip"

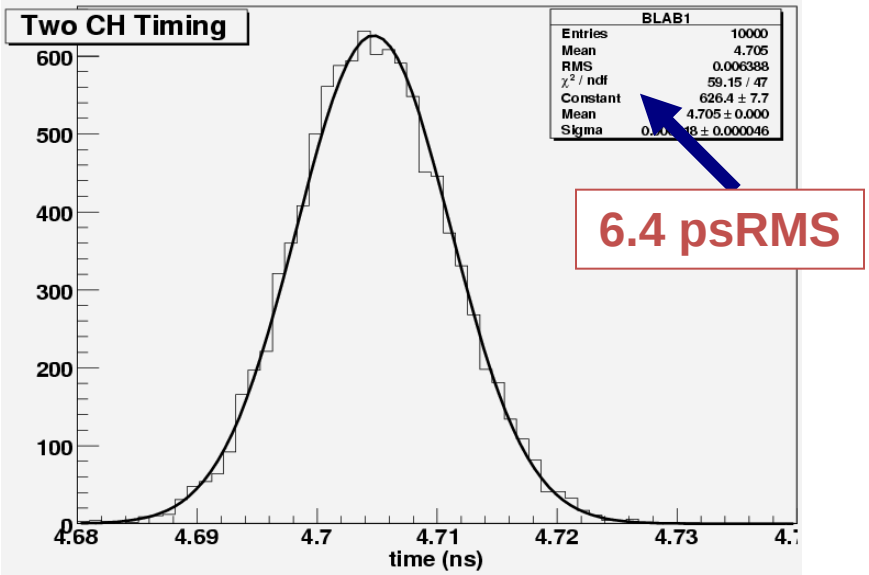
- Comparable performance to best CFD + HPTDC
- MUCH lower power, no need for huge cable plant!
- Using full samples reduces the impact of noise
- Photodetector limited

NIM **A602** (2009) 438





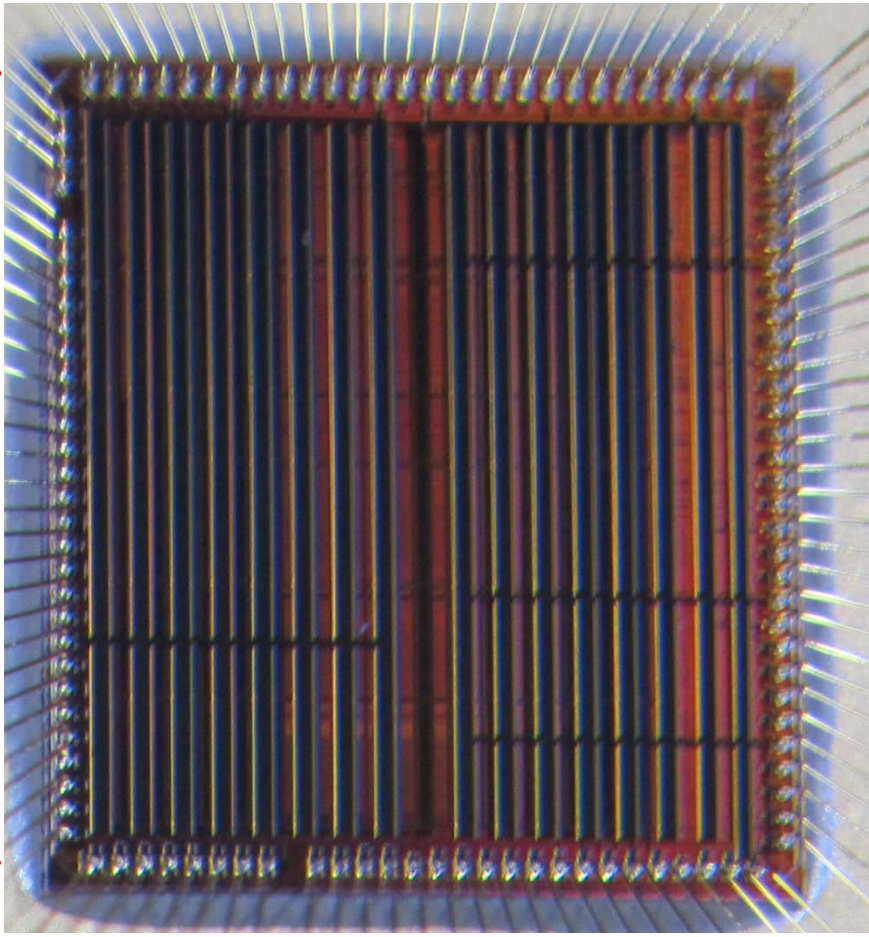




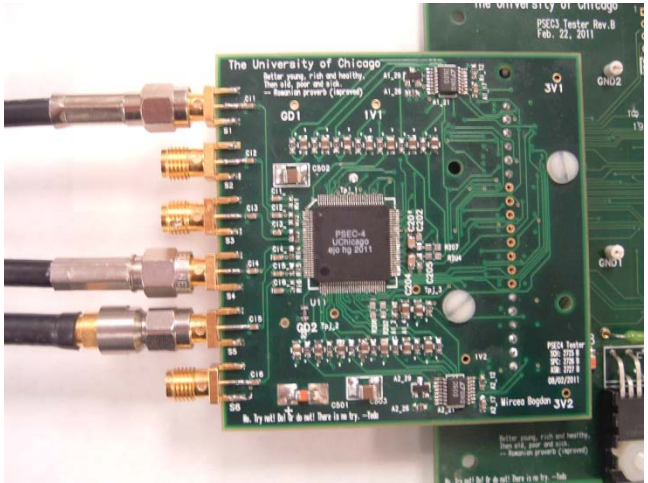
PSEC ASICs

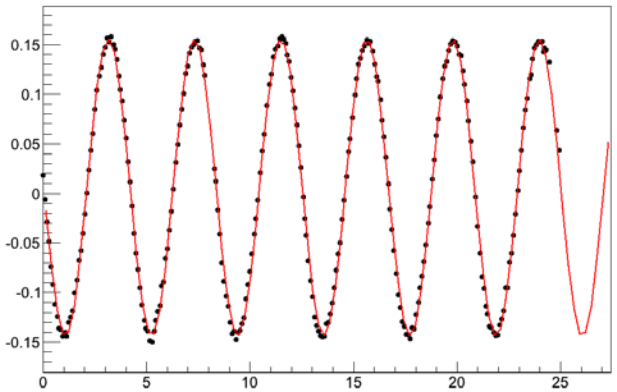
Sampling Rate	2.5 GSa/s-17GS/s
# Channels	6 (or 2)
Sampling Depth	256 (or 768) points
Sampling Window	Depth*(Sampling Rate)$^{-1}$
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz
ADC conversion	Up to 12 bit @ 2GHz
Latency	2 µs (min) – 16 µs (max)
Internal Trigger	yes

4.3mm



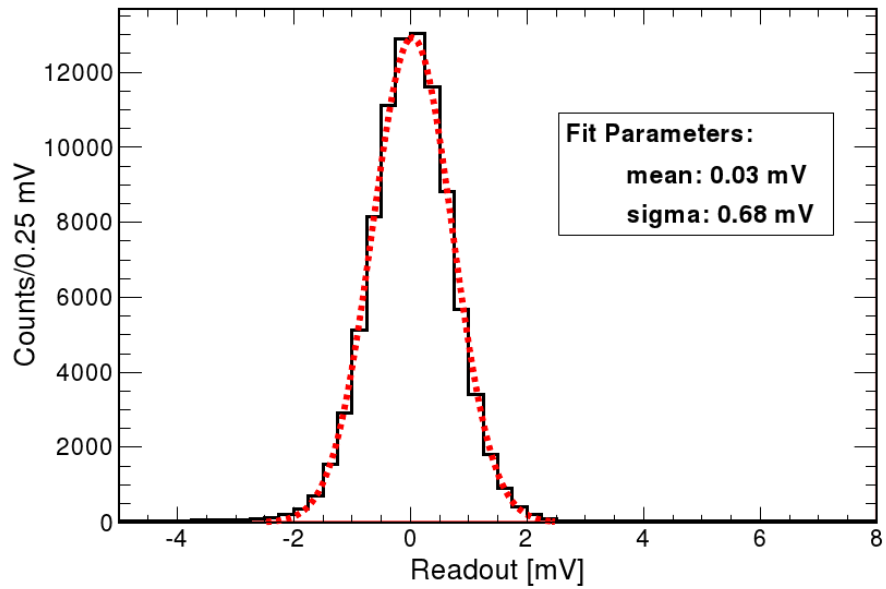
4.0mm

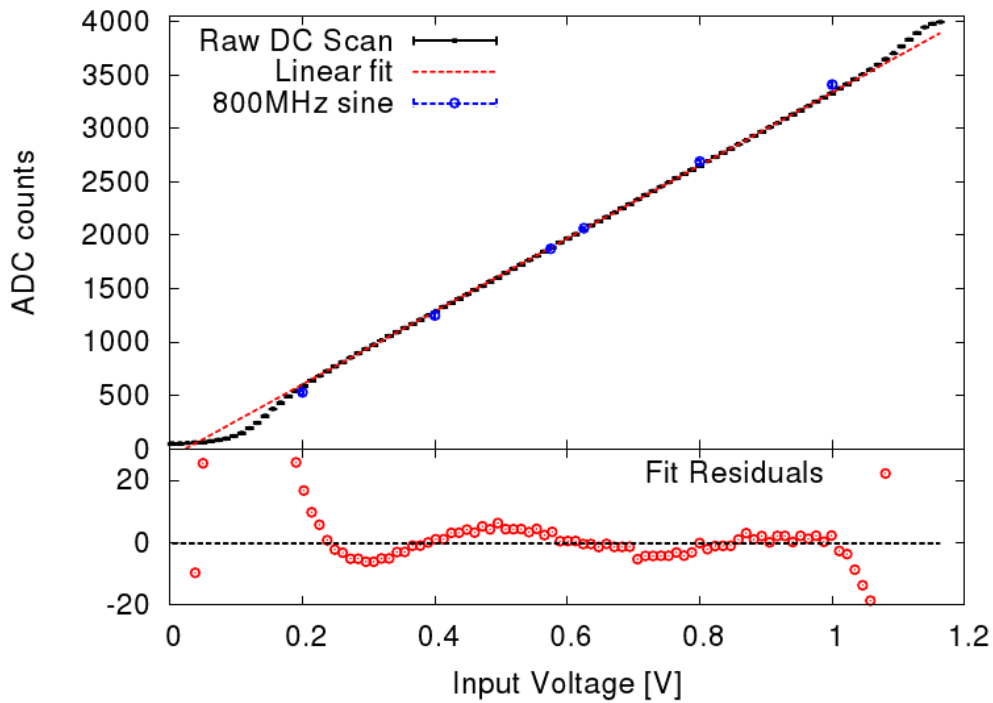


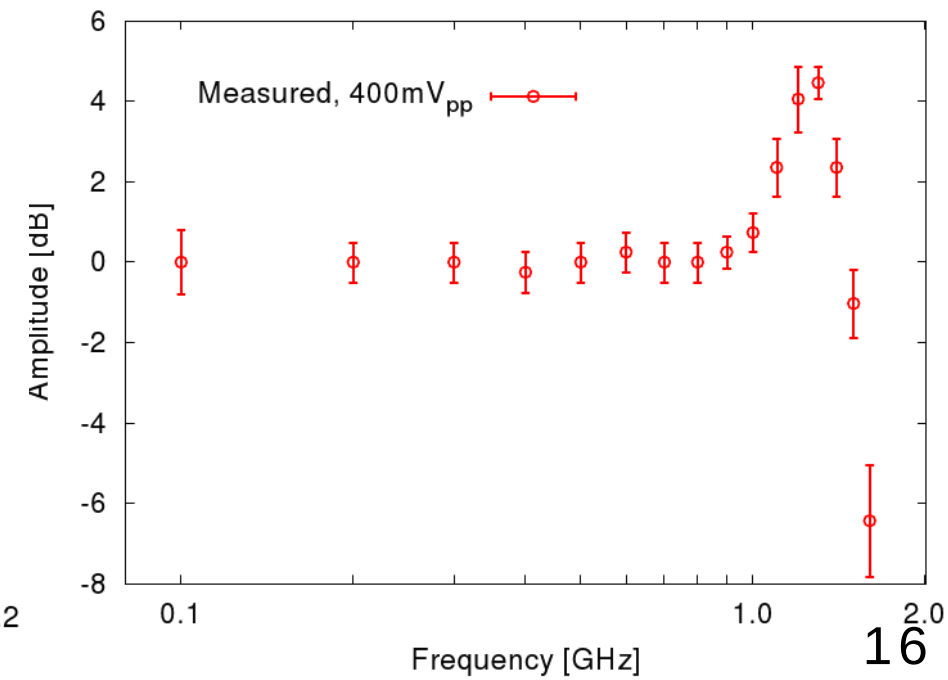


PSEC: Noise, linearity, bandwidth

- **Excellent Performance**
- SNR > 100 possible while maintaining dynamic range
  - → PSEC-4 improvements







Portfolio of options, leading the way

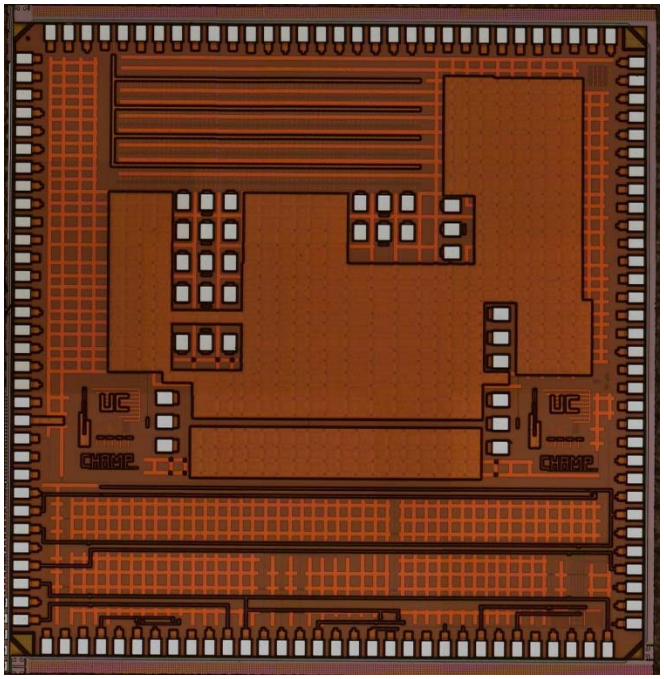
ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

➔ **Success of PSEC: proof-of-concept of moving toward smaller feature sizes.**

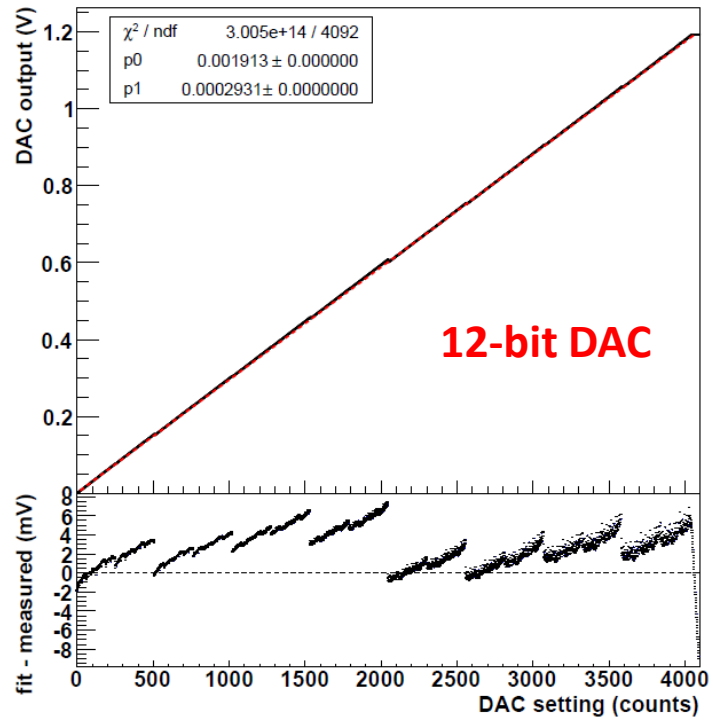
- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

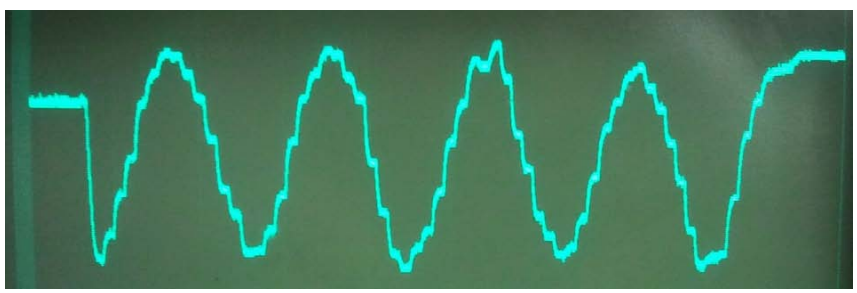
Chicago Hawaii ASIC, Multi-Purpose (CHAMP)

- Developed new circuit elements, trained additional students in the IBM 130nm process

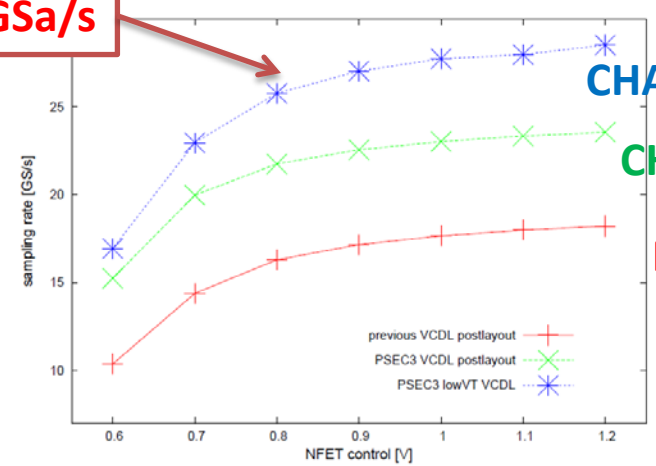


Many useful building blocks, will allow increased functionality, more compact implementation





25GSa/s

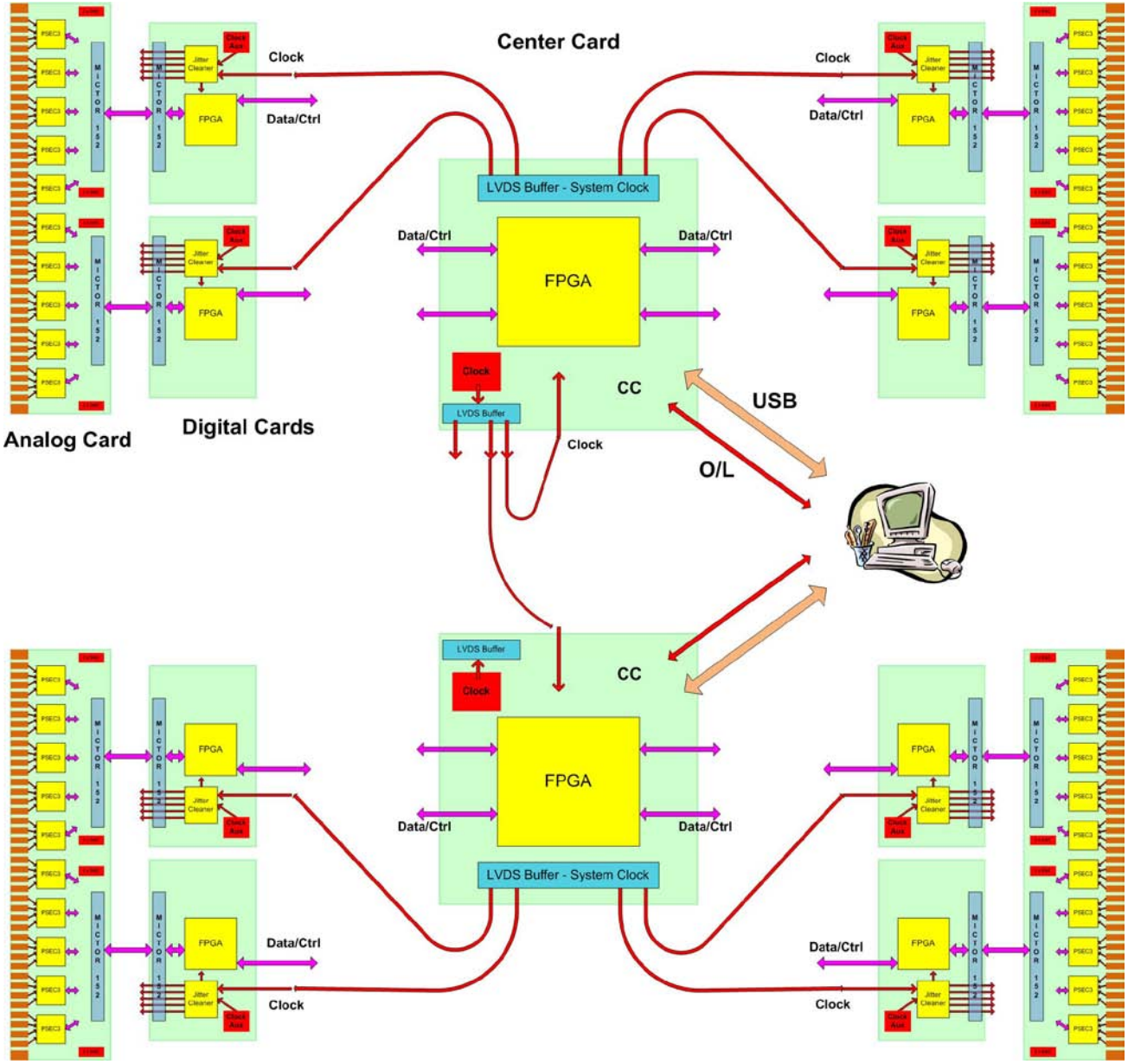


CHAMP low V_t VCDL

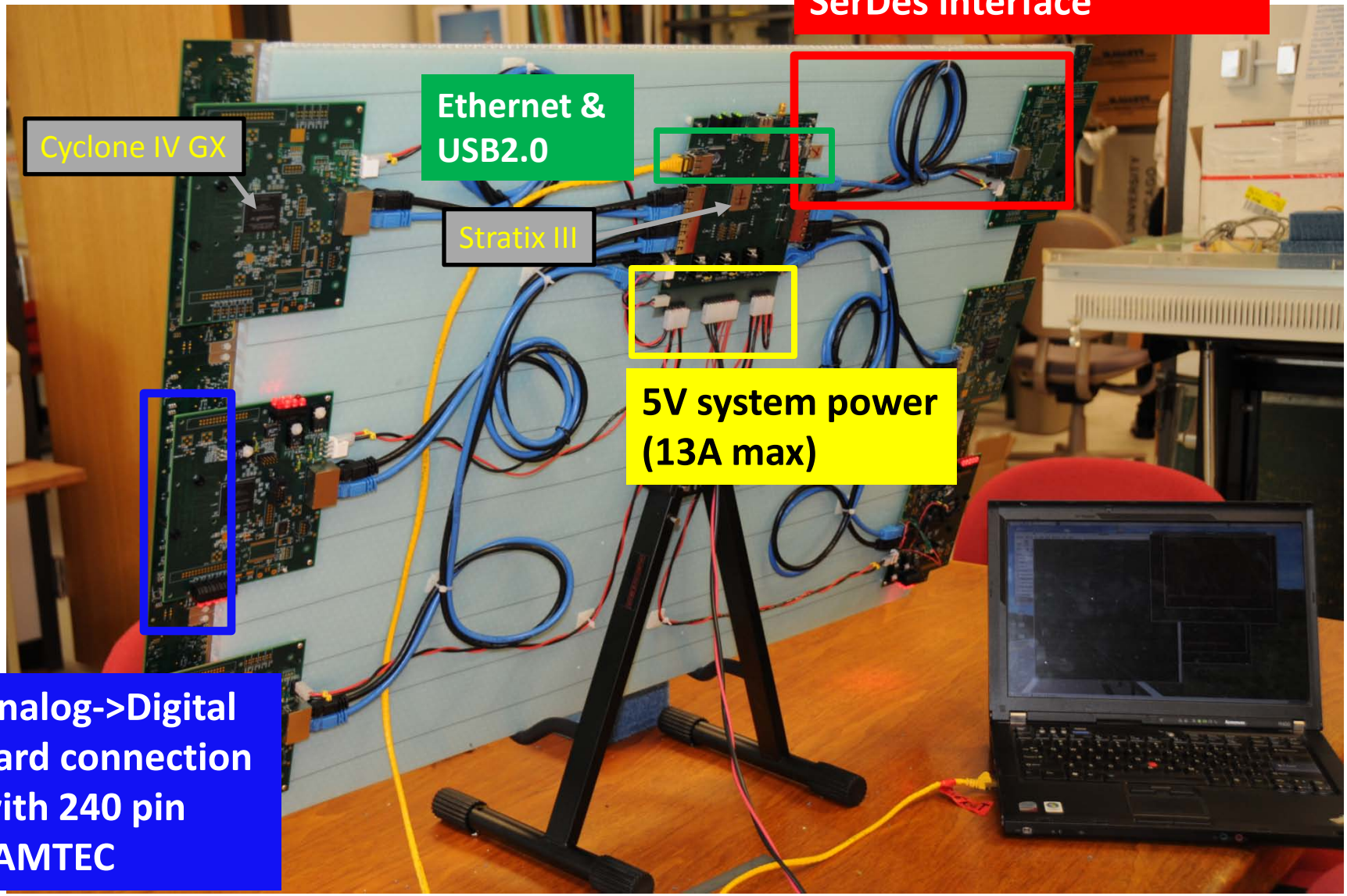
CHAMP VCDL

PSEC3 VCDL

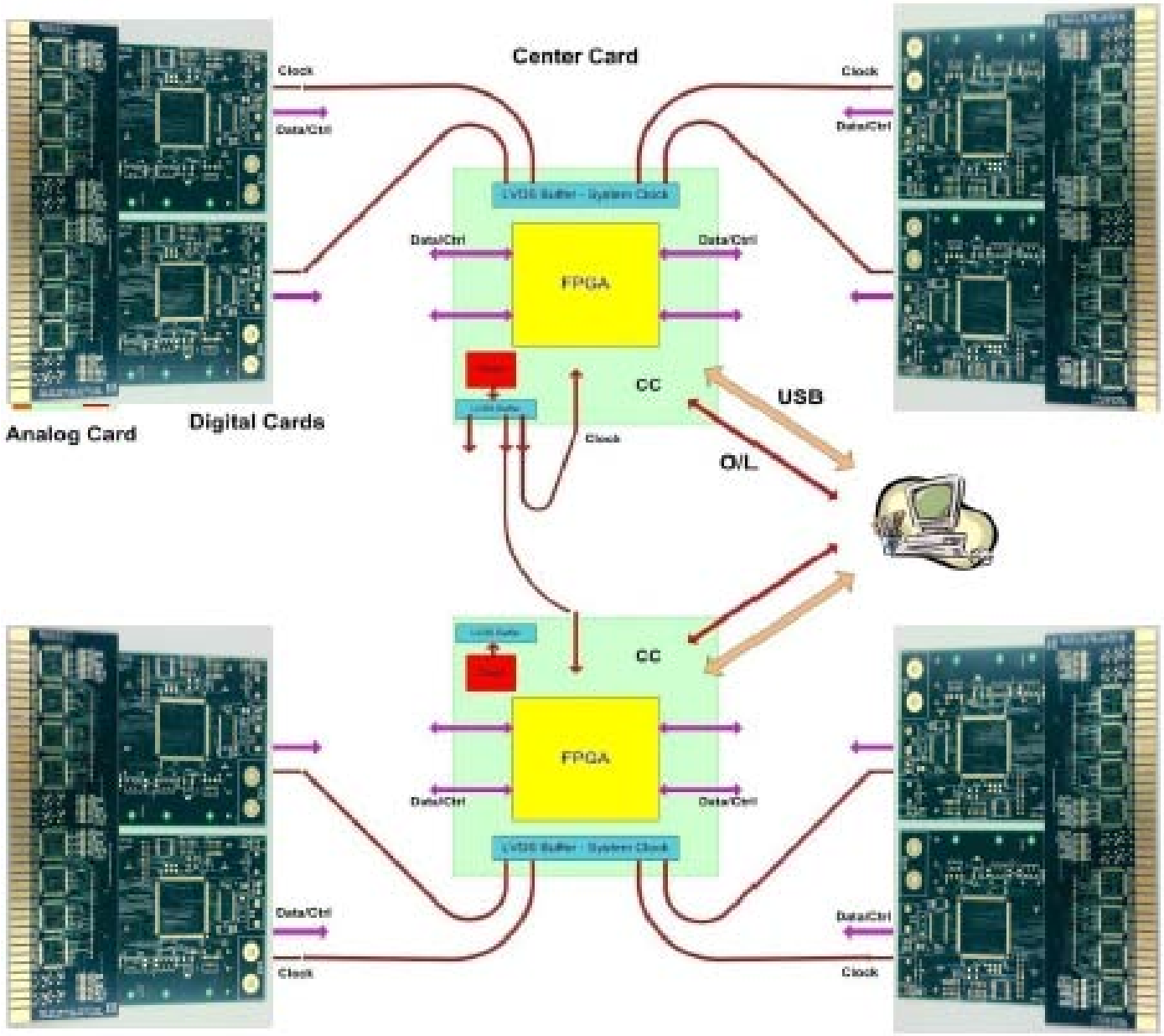
Readout System, beam test configuration



Super Module: features



Readout System, beam test configuration

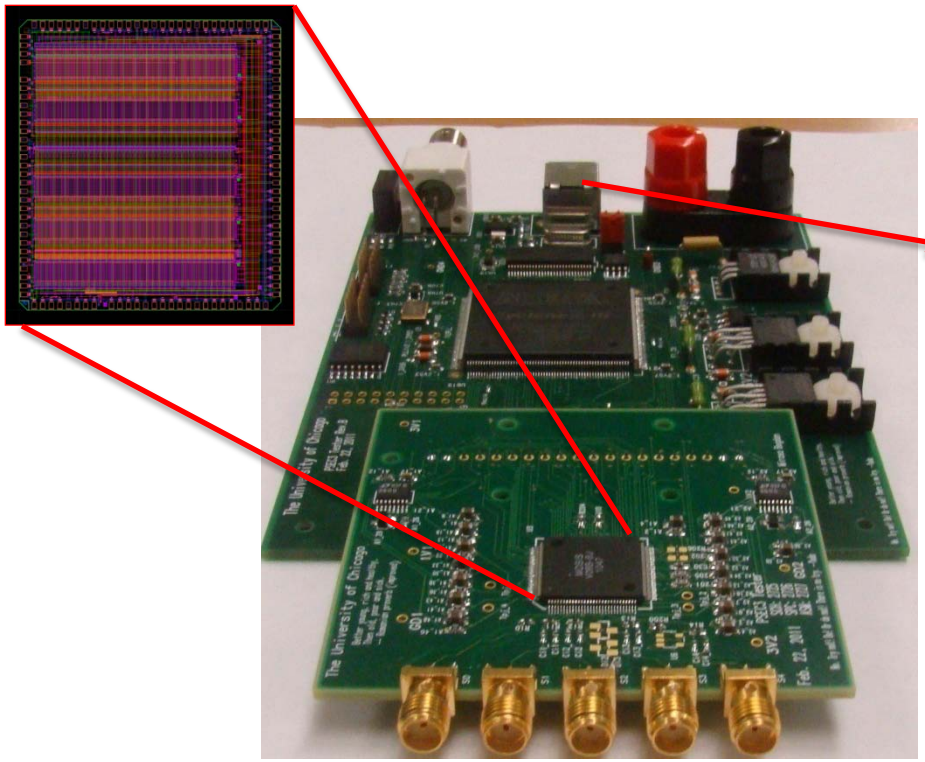


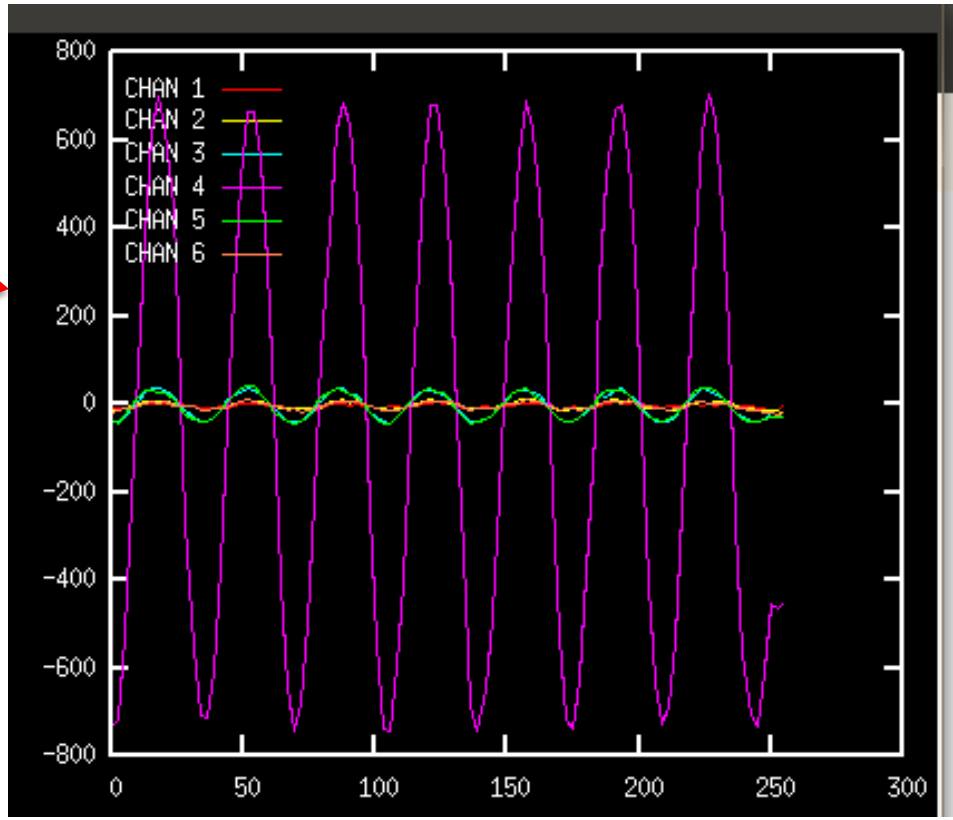
Respin Analog card only for different ASIC

A variety of data collection configurations possible

Demonstrate timing distribution @ ps level between modules

Oscilloscope on a chip?





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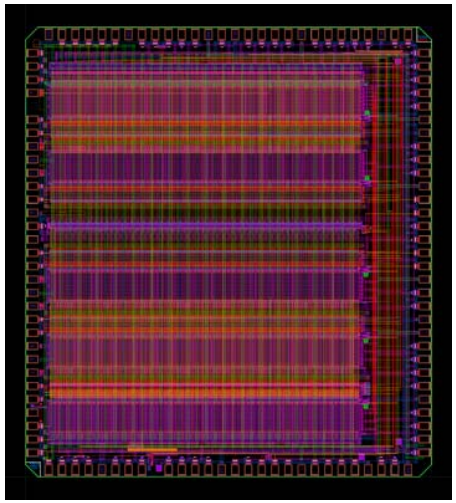
Oscilloscope on a chip? ➔ Calibration

- Modified approximation:



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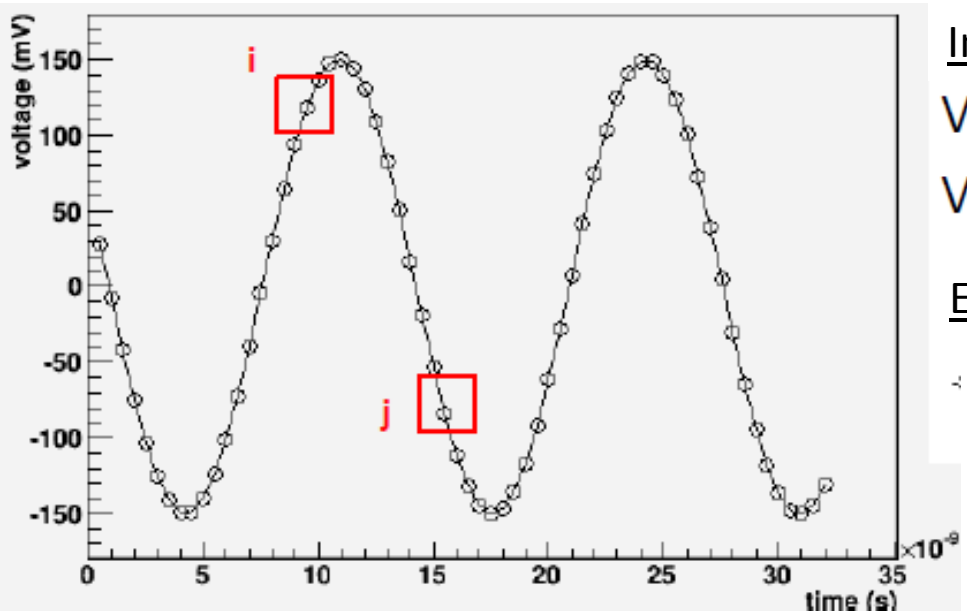
Timing Calibration w/ Correlations

- Plot correlations between pairs of samples:
  - To determine Δt_{ij}, plot $V_i - V_j$ versus $V_i + V_j$



Input signals given by:

$V_i = A \sin(\omega t_i + \phi)$

$V_j = A \sin(\omega t_j + \phi)$

Effectively rotate by 45±:

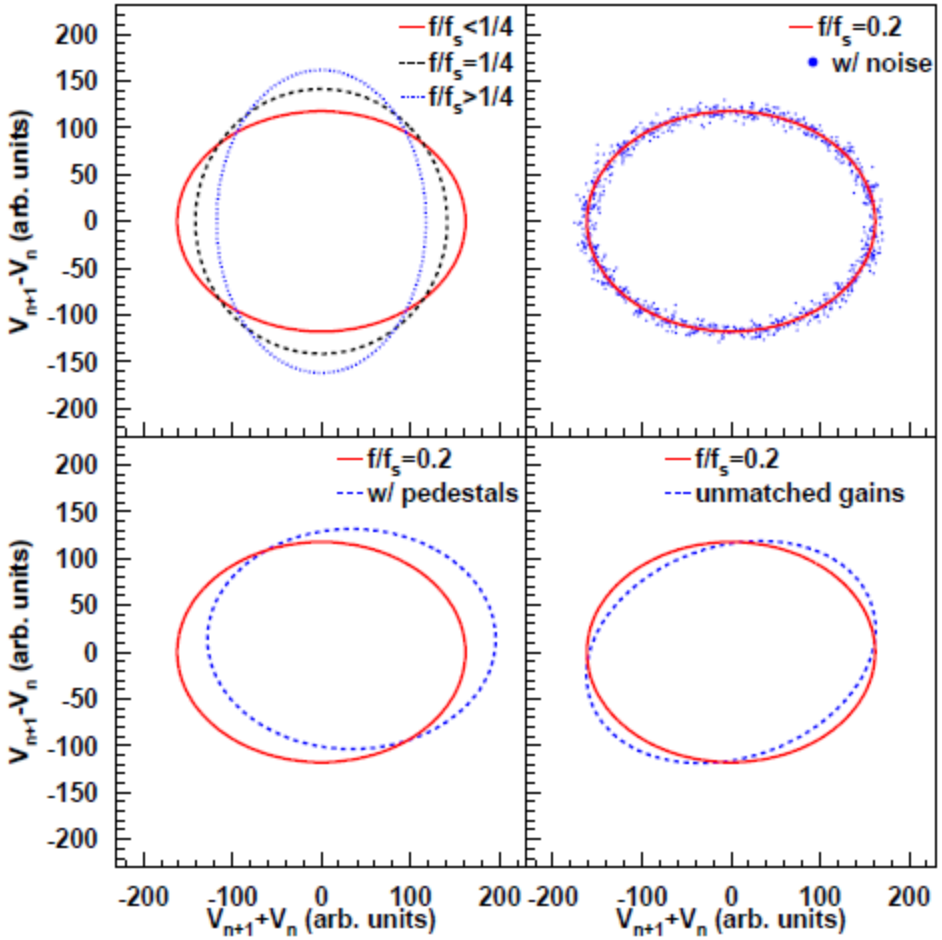
- $x := V_i + V_j$
- $y := V_i - V_j$

➔ $$\frac{x^2}{4A^2\cos^2(\omega\delta t/2)} + \frac{y^2}{4A^2\sin^2(\omega\delta t/2)} = 1$$

- **i and j can be adjacent (or not), but cycle ambiguities exist if > 1 period apart.**

Timing Calibration w/ Correlations

- Ellipse features:



1) Different Δt (for known sampling frequency) give different major/minor radii.
2) Noise makes ellipse "fuzzy"
3) Nonzero pedestals shift origin
4) Difference in gain between two cells causes a rotation.

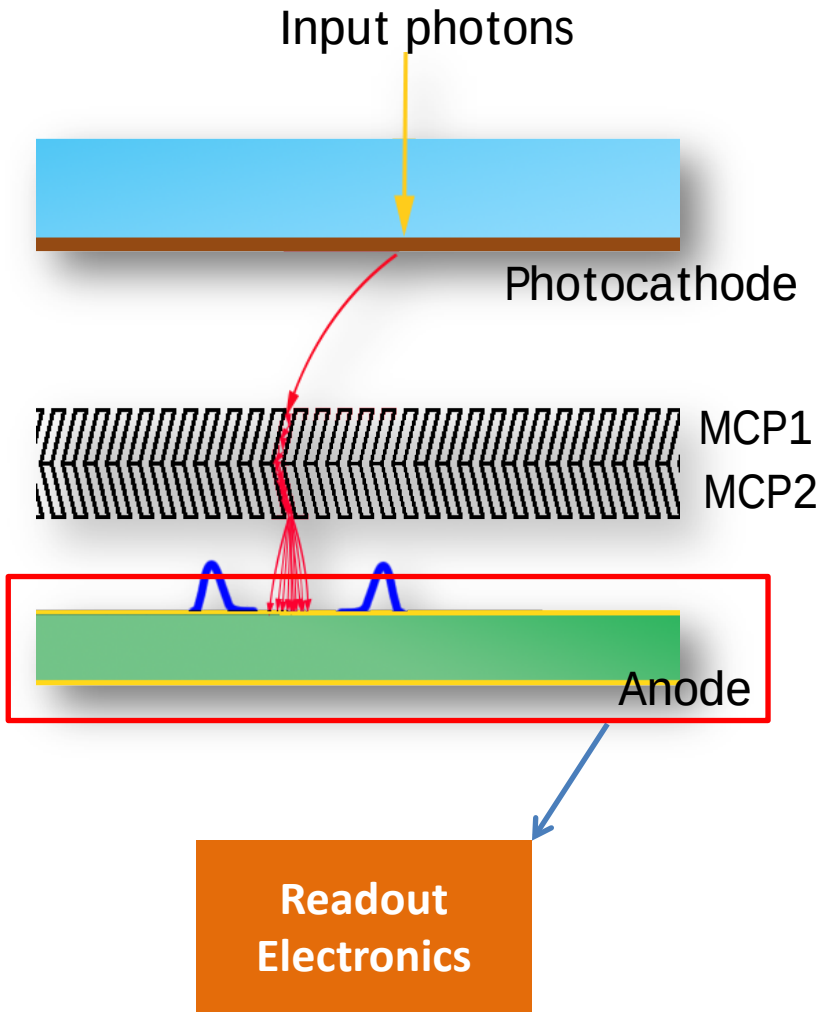
➔ We have written an ellipse fitter to perform this method.
➔ Even without fitting, it provides nice qualitative check on results.

- **Far more efficient than other methods**

Many highlights

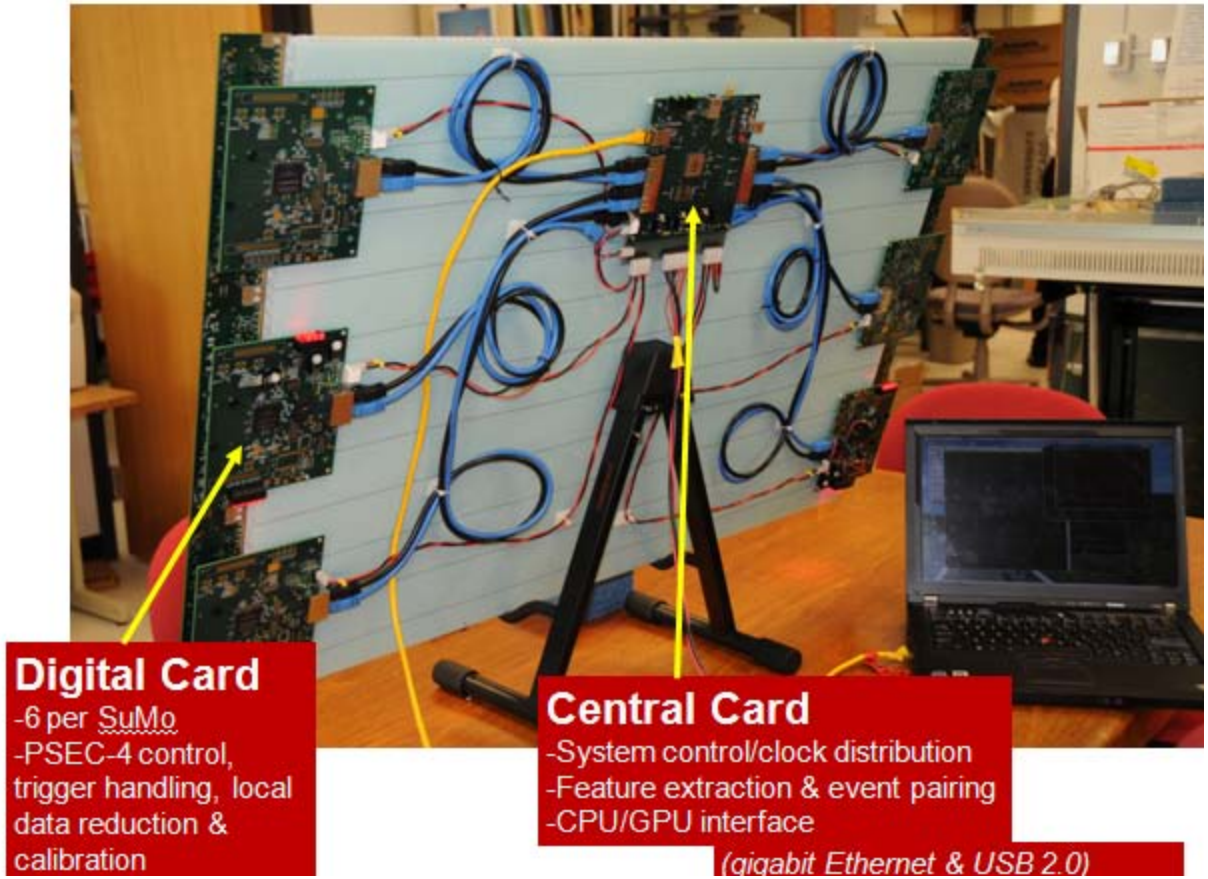
1. Clarifying processes that limit timing resolution: http://psec.uchicago.edu/workshops/fast_timing_conf_2011
2. Charge signal coupling into the readout anodes
3. Optimizing electro-mechanical integrated readout
4. Impressive results with the PSEC ASICs
5. Developed expertise with the IBM 130nm process, tested future subcircuits on the CHAMP ASIC
6. ASIC evaluation boards, first tile/module scale readout
7. Options for large-scale/high-speed readout explored, a number of application-specific ASIC solutions identified
8. Refining of calibration procedures, required constants, and data reduction

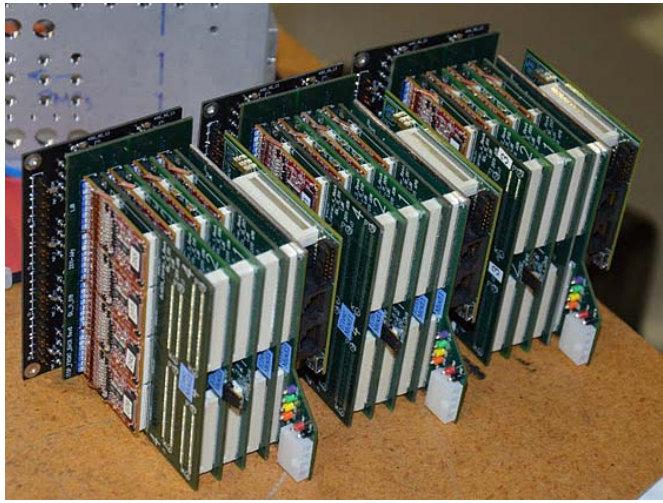
Are we done?


Input photons
Photocathode
MCP1
MCP2
Anode
Readout Electronics

NEW HOUSE. NEW FAMILY.
WHAT COULD POSSIBLY GO WRONG?
ICE CUBE
ARE WE DONE YET?
APRIL 2007

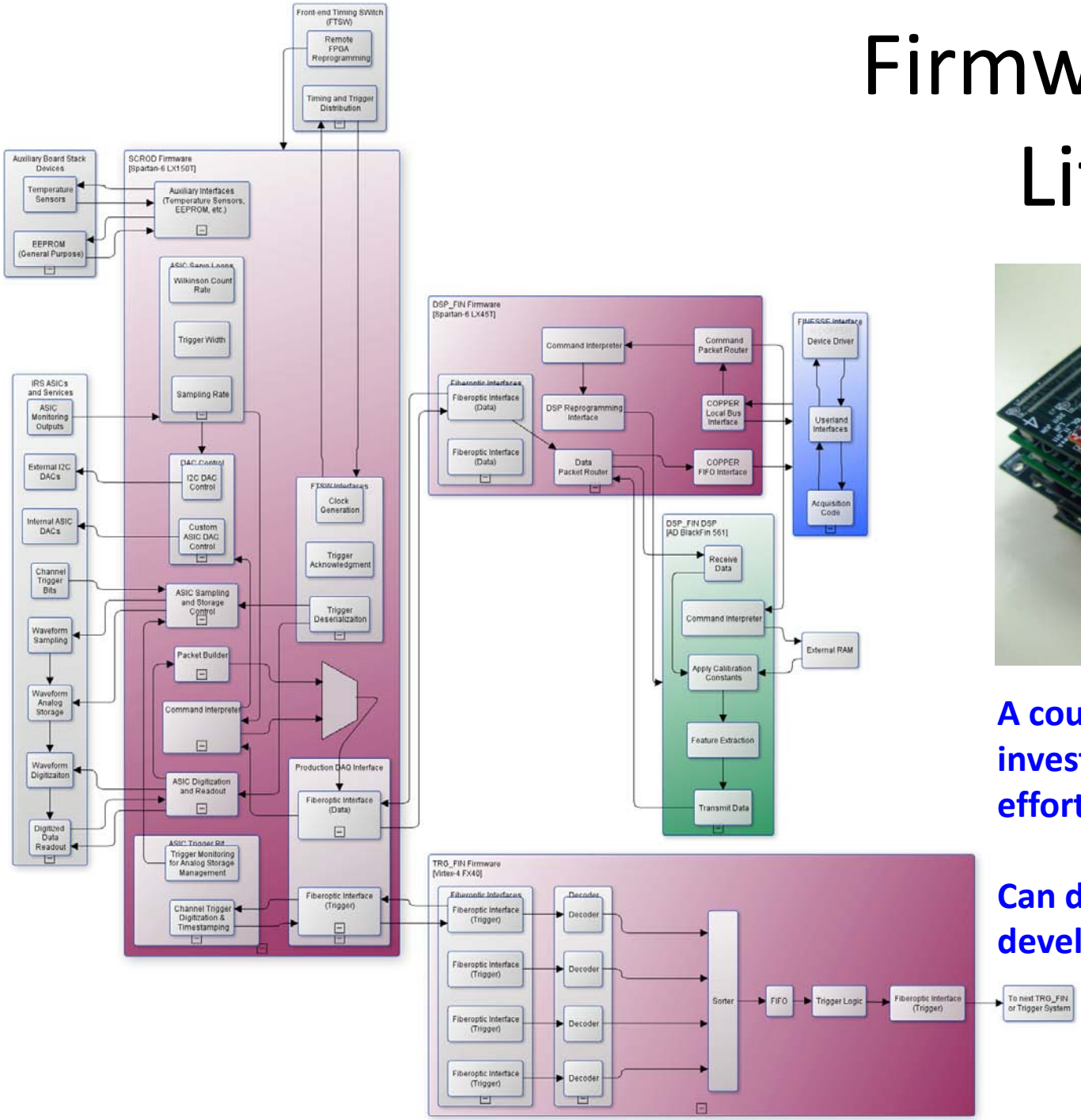
System Engineering Issues

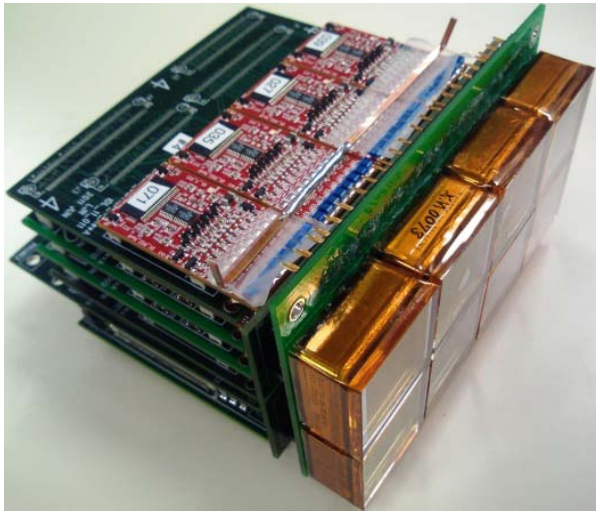




- **Current experience with Belle II iTOP development → much firmware/infrastructure development required still**

Firmware Heavy Lifting…





A couple of man-years already invested in firmware – much effort put into infrastructure

Can directly benefit from this development effort

Firmware Heavy Lifting (part II)

Electronics Instruction Set

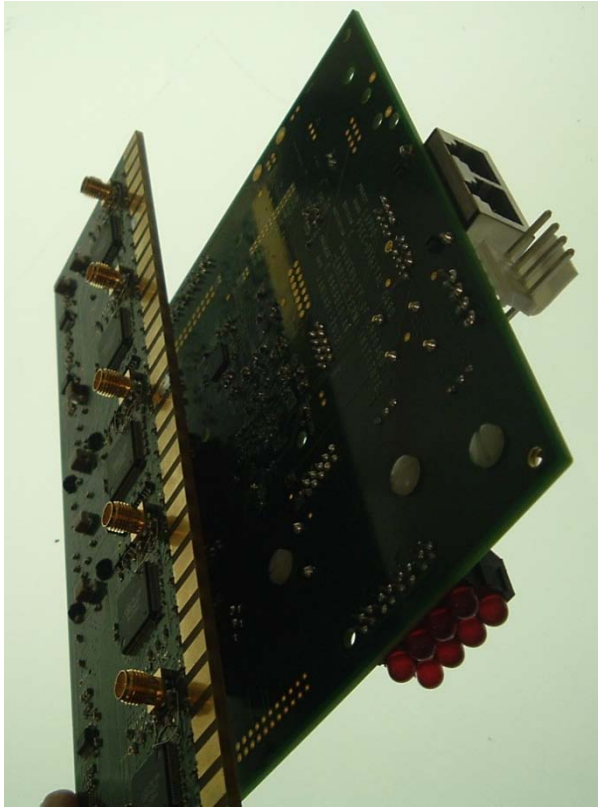
The electronics use a fixed-width 48 bit instruction set. The first 4 bits are the next 6 bits are the channel mask, the next 11 bits are options, and the last 16

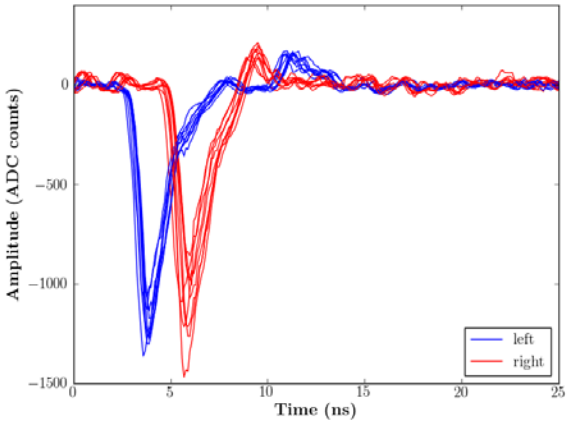
INS	DC	PSEC4	CHAN	OPTS	VAL
0010	001111	01110	111111	000000000000000	000000000000

would acquire the data from the 18 central channels on each analog card.

List of instructions.

Name	Hdr	Opts	Purpose
No-Op	0x0	NULL	Does nothing.
Trigger	0x1	NULL	Tells the PSEC to collect data.
Acquire	0x2	NULL	Tells the DC to pass PSEC data to DC.
Raw Read	0x3	NULL	Read the raw DC data to the CC.
Evt Read	0x4	NULL	Read the event DC data to the CC.
Get Evts	0x6	NULL	Reads VAL CC events from the CC FIFO to the PC.
Set	0x5	*	Sets pedestal and calibration values on the AC.
Reset	0xF	*	Resets components specified by opts.

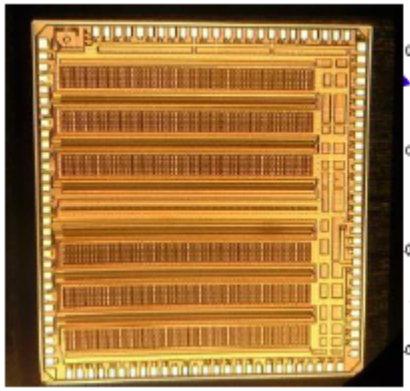


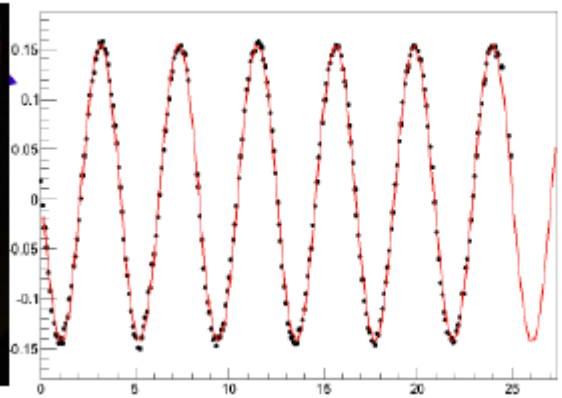


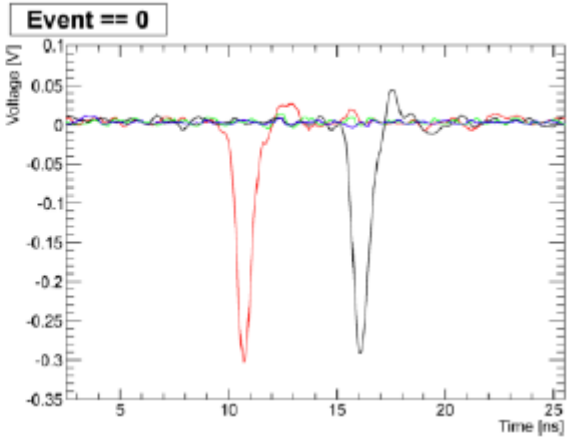
SuMo system firmware – basic structure in place

A significant amount of work still needed

PSEC5 ?







- PSEC-4 has demonstrated excellent performance:
  - Demonstrator of waveform sampling in 130 nm CMOS.
  - Sampling rate $\geq$ 10 GSa/s.
  - Analog bandwidth $\geq$ 1 GHz.
- Main drawback:
  - Buffer is only 256 samples long (~25 ns @ 10 GSa/s).

– Applications discussed:

- TOF PET
- Next generation water Cherenkov
- Hadron collider precision TOF
- KOTO preshower calorimeter

Applications demanding the best (~1 ps) timing.

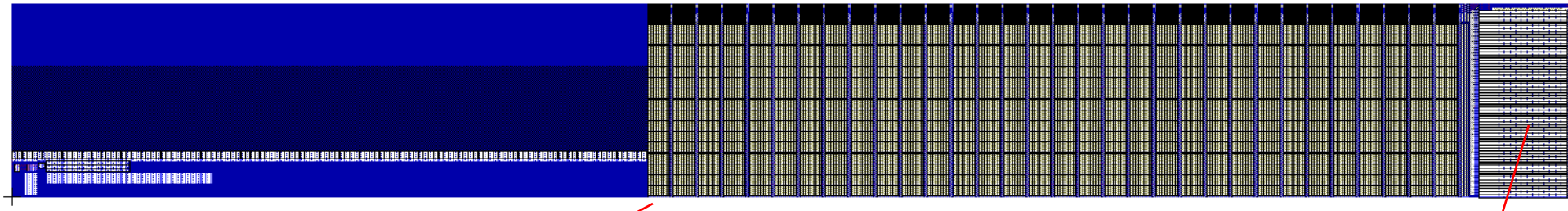
Specifications similar enough that a single ASIC (PSEC-5) could be suitable.

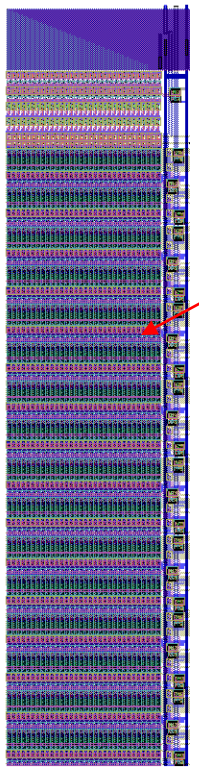
"2 stage transfer" Architecture of IRS/TARGET ASICs demonstrated

2-stage transfer

- Sampling: 128 (2x 64) separate transfer lanes

Recording in one set 64, transferring other ("ping-pong")





- Concurrent Writing/Reading
- Only 128 timing constants
- Storage: 64 x 512 (512 = 8 * 64)
- Wilkinson (64x1))
- 64 conv/channel

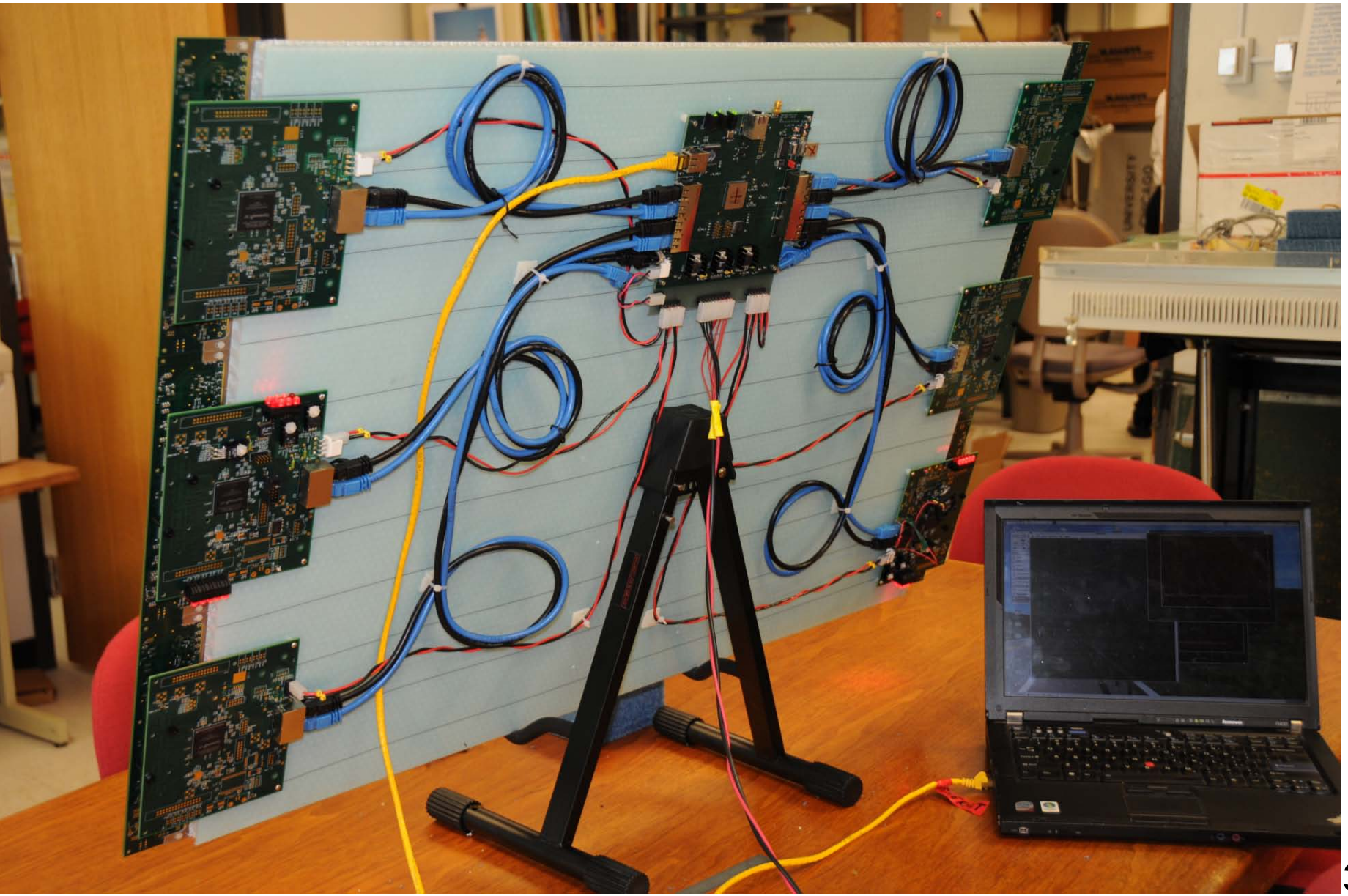
Need for Electronics Support

- Efforts to date university based
- Our CAD tools licenses do not allow commercial sale of designs
- Longer term solution – engage industry, National Labs
- Building toward full system deployments with first adopters

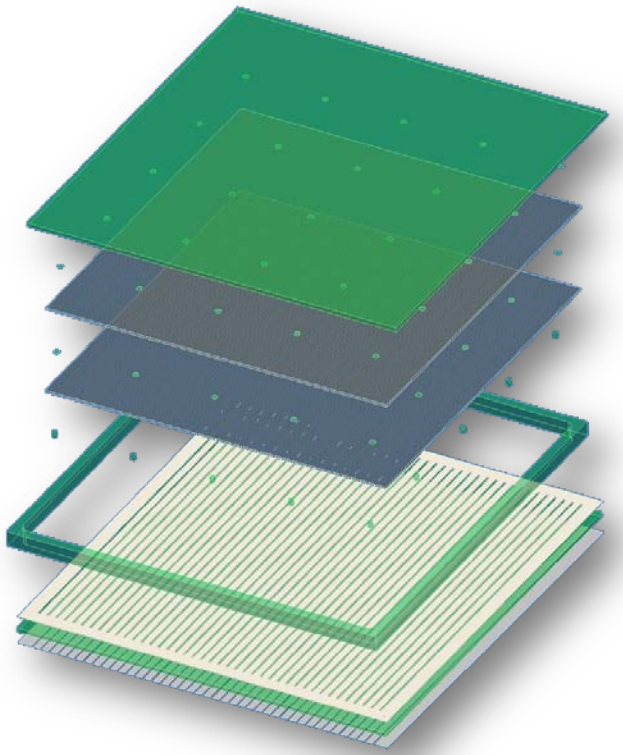
Electronics Summary

- Steady progress, resource (human) bounded
- Are learning much from first integrated readout tests
- Experience operating readout systems at ANL, Chicago, Hawai'i and SSL
- Still room to improve (e.g. PSEC5)
- Longer-term support, 2 paths: commercialization, National Labs

Backup



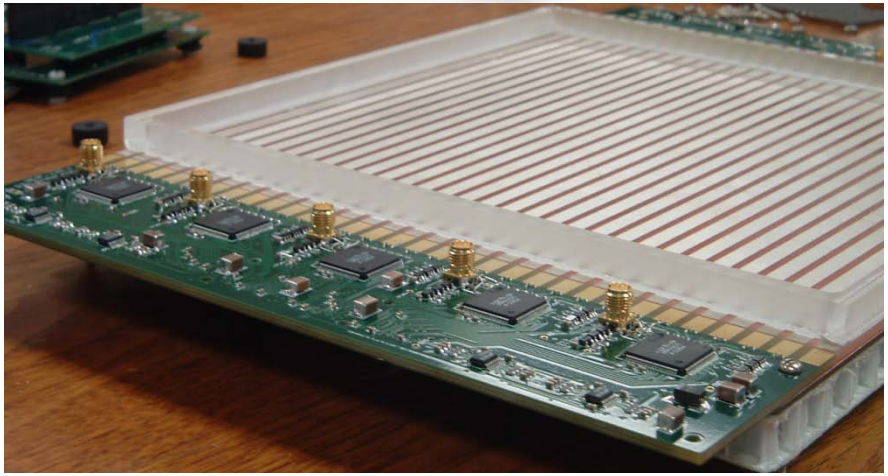
Coupling Electronics to Large Area MCPs



Large Area MCP structure:

- Custom photo-cathode
- 2-plate chevron (high gain)
- **Transmission line 2D readout**

(limit the number of electronics channels)



Electronics:

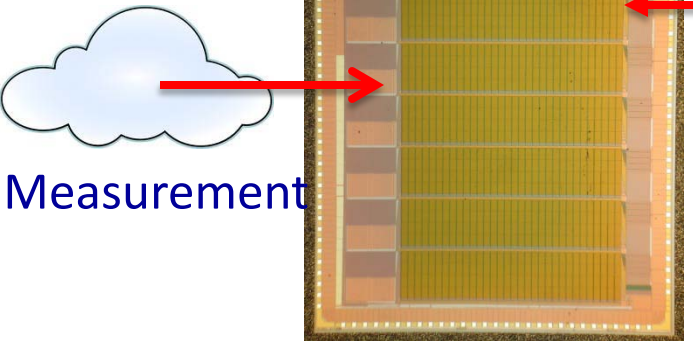
- **GSa/s Waveform Sampling + Signal processing**

A “Giga” Overview (Modern Readout)

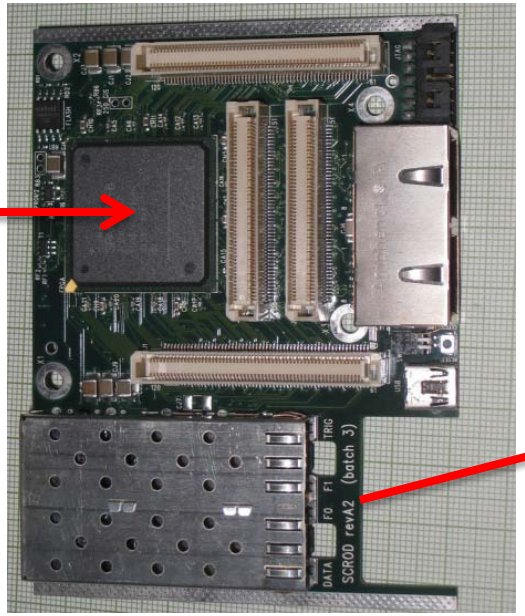
2. 100’s of **Giga**flops per Field-Programmable Gate Array

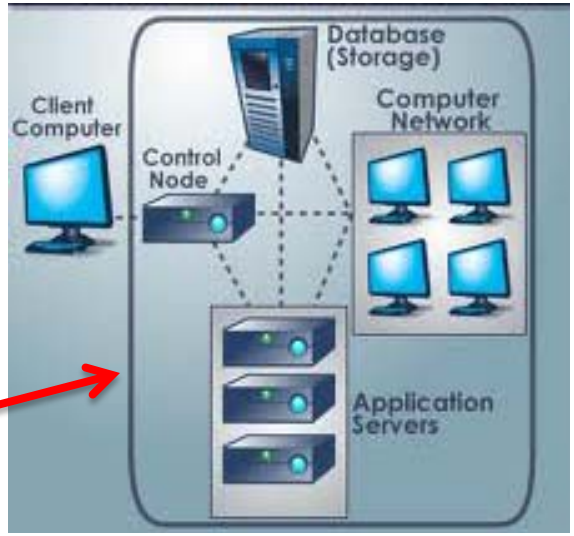
4. Commodity Servers running at **Giga**-Hz rates, 1000’s of **Giga**flops

Physical



Measurement





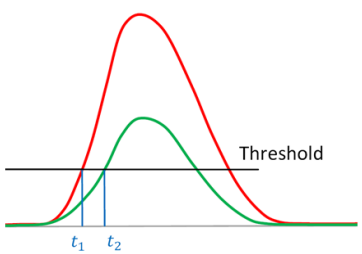
1. **Giga**sample/s “digital oscilloscope on a chip”

3. Inexpensive **Giga**-bit/s fiber link interconnect; **Giga**-bit ethernet

Technology advances ➔ high rate, high-precision experiments

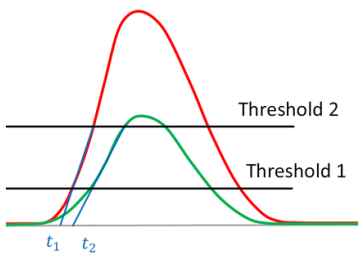
Timing Extraction Methods

Single threshold



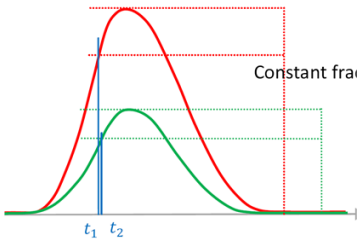
The single threshold is the least precise time extraction measurement. It has the advantage of simplicity.

Multiple threshold



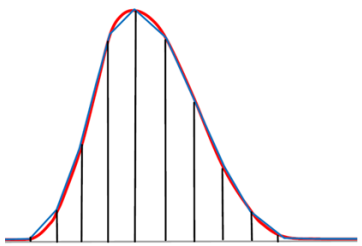
The multiple threshold method takes into account the finite slope of the signals. It is still easy to implement.

Constant fraction



The constant fraction algorithm is very often used due to its relatively good performance and its simplicity.

Waveform sampling



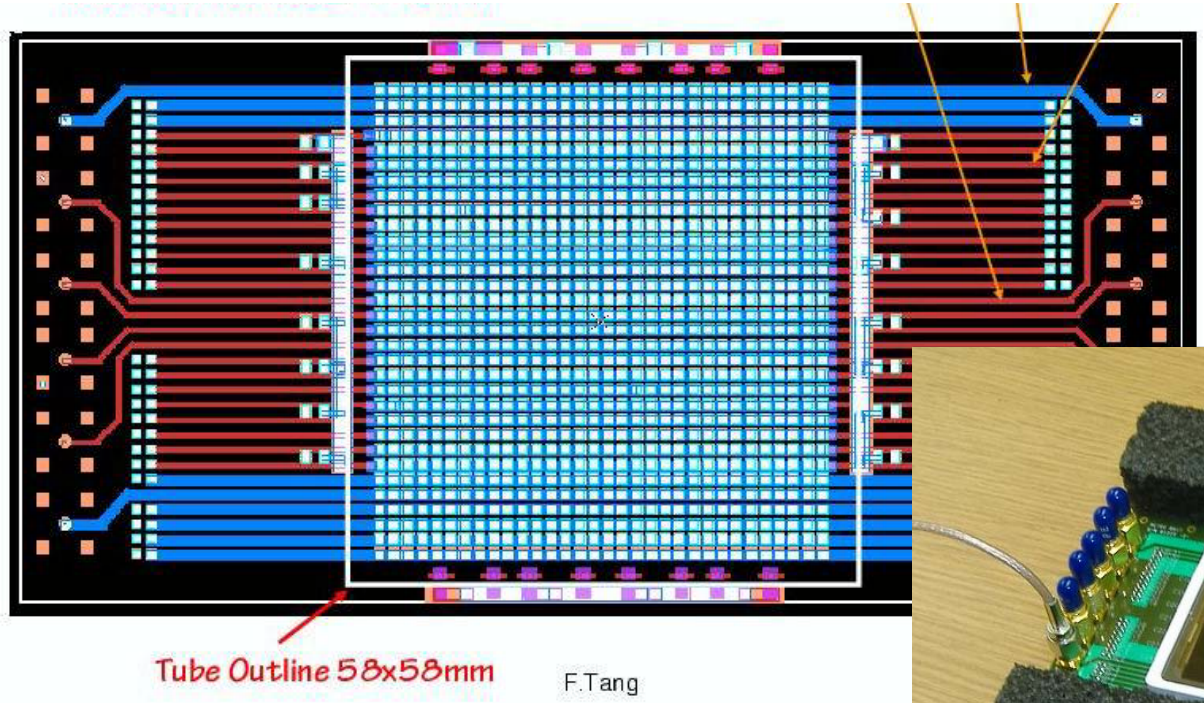
The waveform sampling above the Nyquist frequency is the best algorithm since it is preserves the signal integrity.

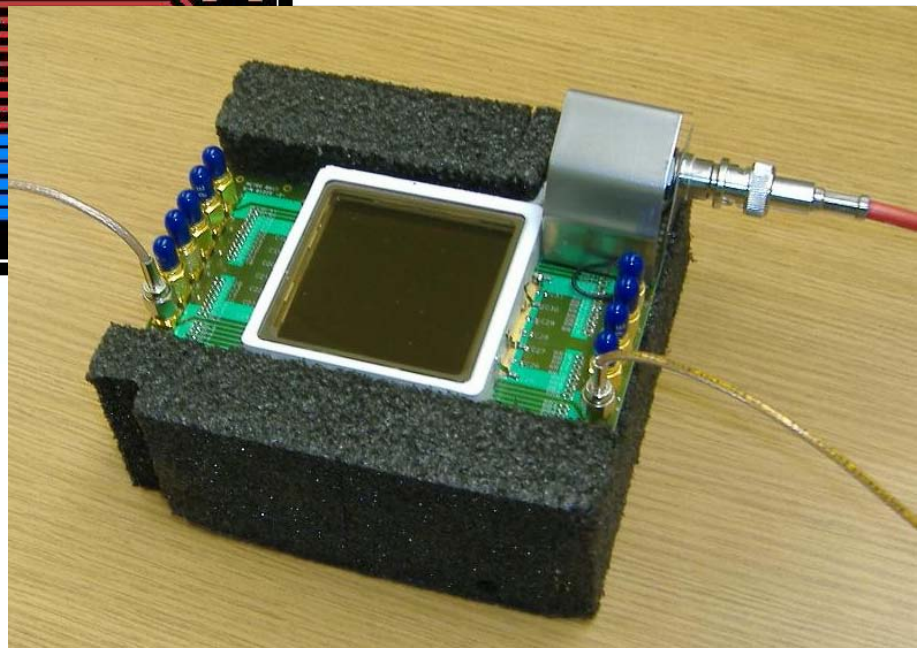
In principle, sampling above the Nyquist-Shannon frequency and fully reconstructing the signal attains the best timing information.

Attrib. Jean-Francois Genat

Stripline Anodes (Prototype)

- Photonis-Planacon on transmission line PCB:



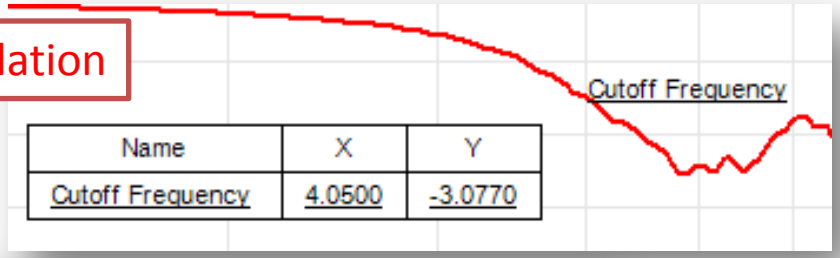


- **Striplines allow coverage of a large area with a manageable number of channels.**

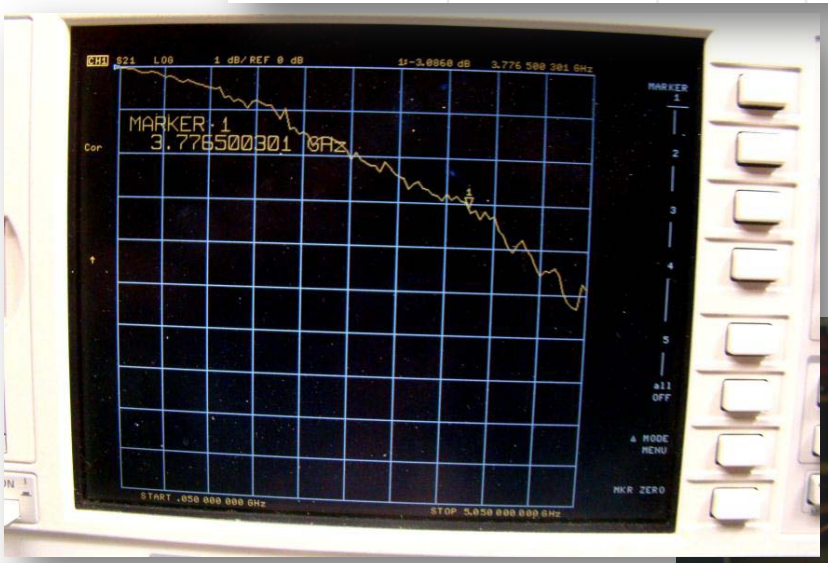
Courtesy Fukun Tang, Greg Sellberg

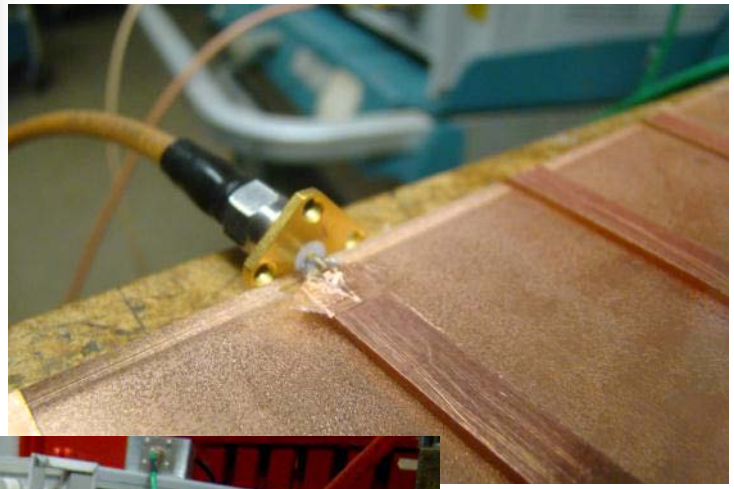
Copper strip testbench

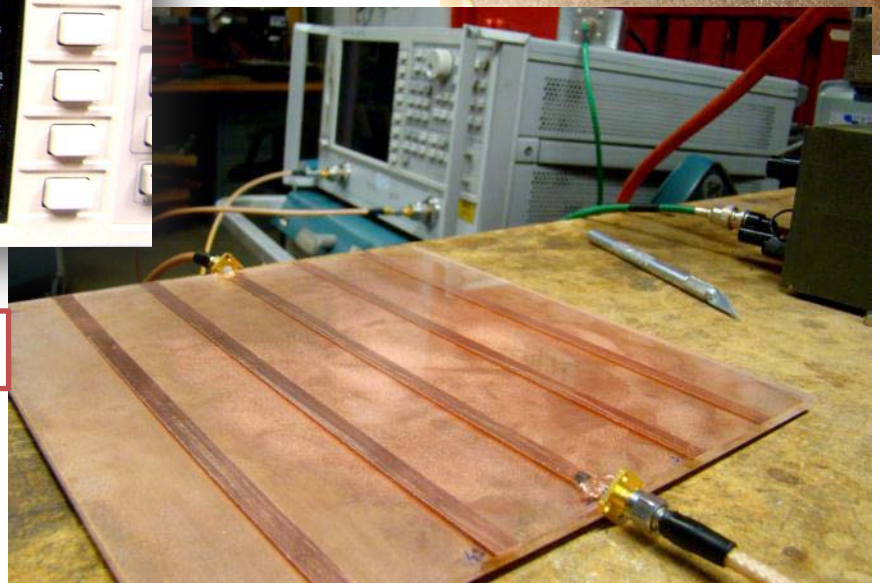
Simulation



Name	X	Y
Cutoff Frequency	4.0500	-3.0770



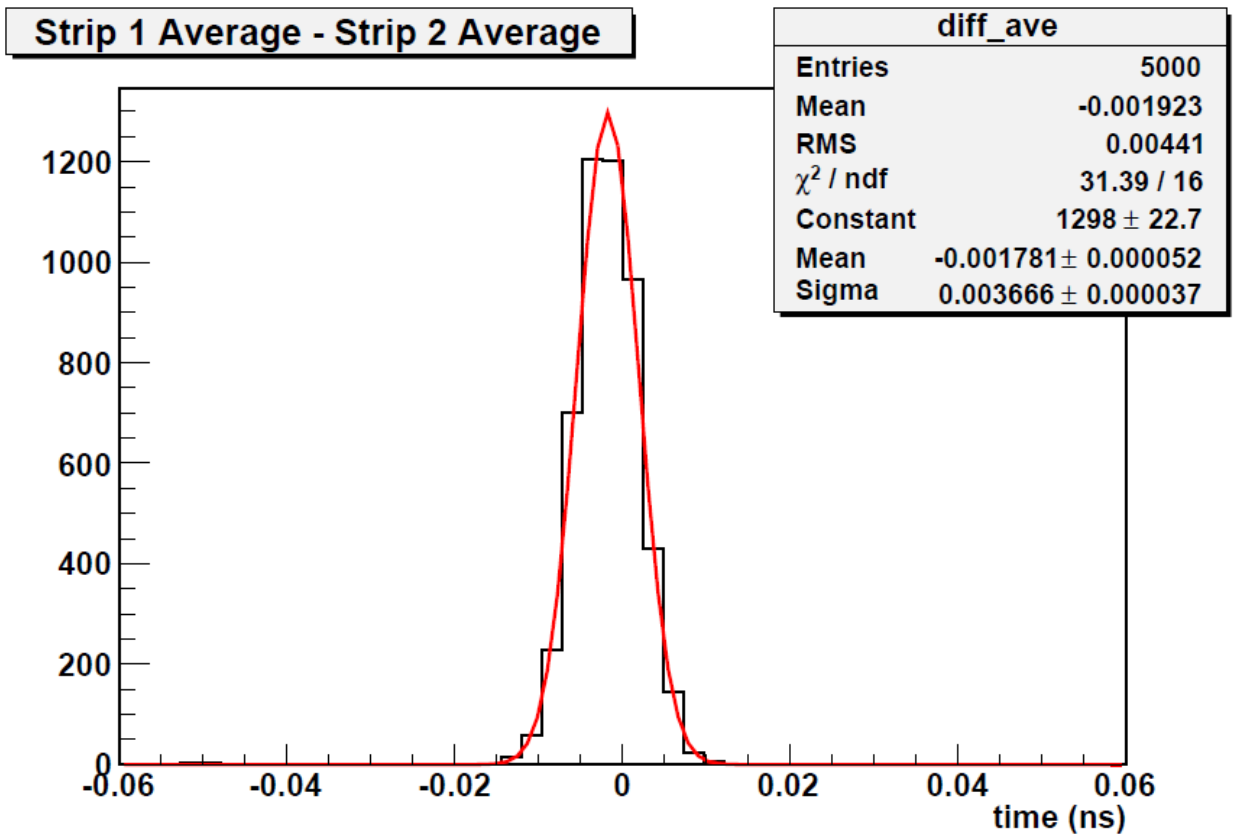




Measurement – good agreement

Stripline Anodes Measurement

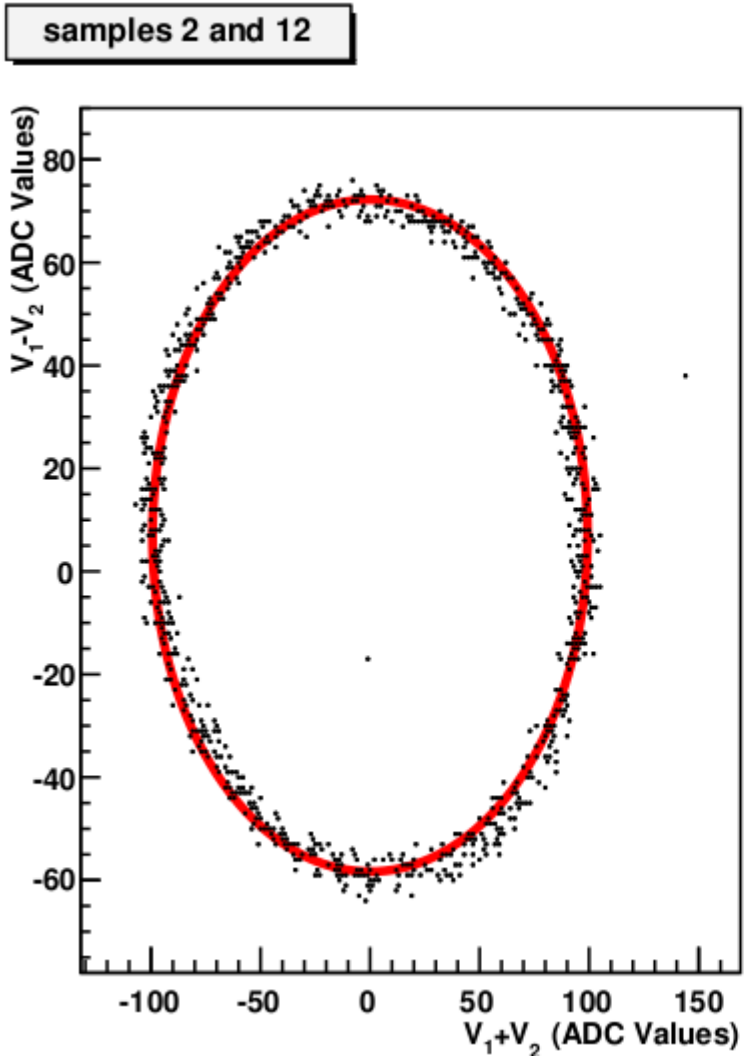
- **Average time ($(t_1+t_2)/2$) along strip gives arrival time**
- **Time difference (t_1-t_2) gives the position**



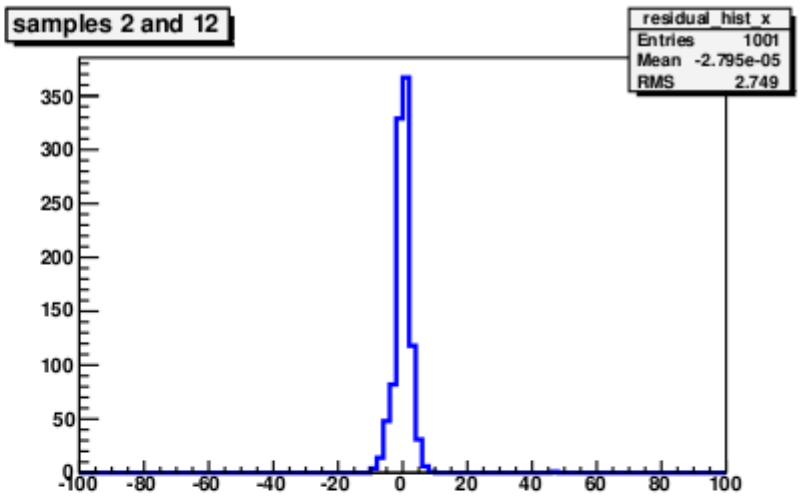
σ_t of order ps feasible for large N_{pe}

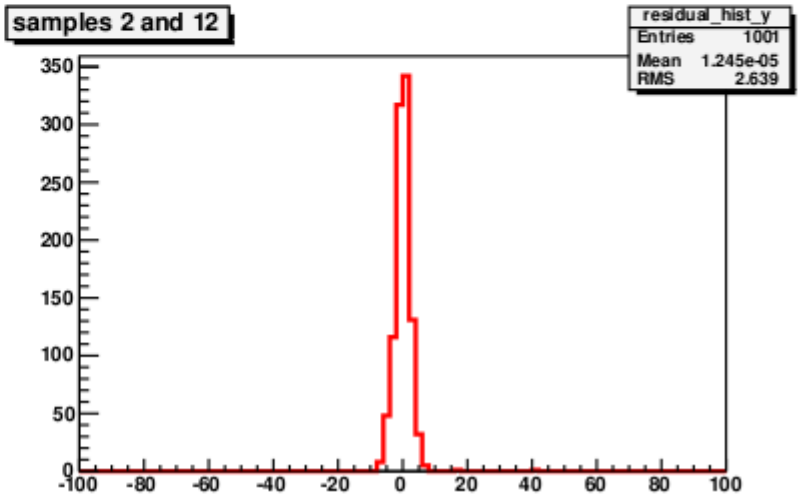
Example Fit w/ PSEC Data

Data and fit



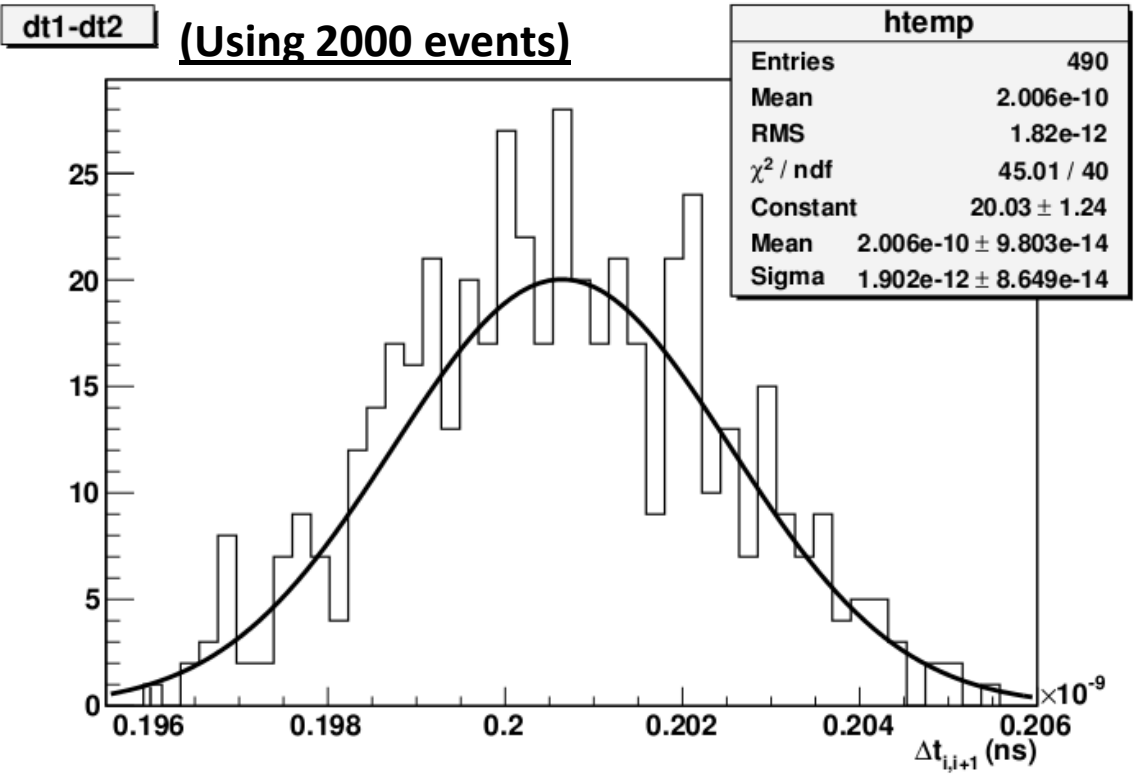
Residuals in x, y





- **Fits are well behaved, converge nicely**

Calculated Δt values for TDS6804B



w/ scope set to 5 GSa/s:

Δt = 200.6 ps

$\sigma_{\Delta t}$ = 1.9 ps

Excellent resolution even with a small dataset.

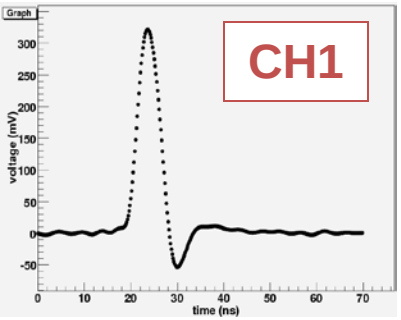
Technique verified… next is PSEC data.

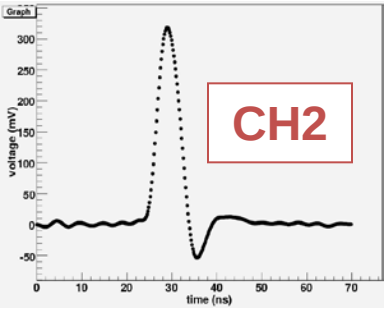
TDS6804B Datasheet

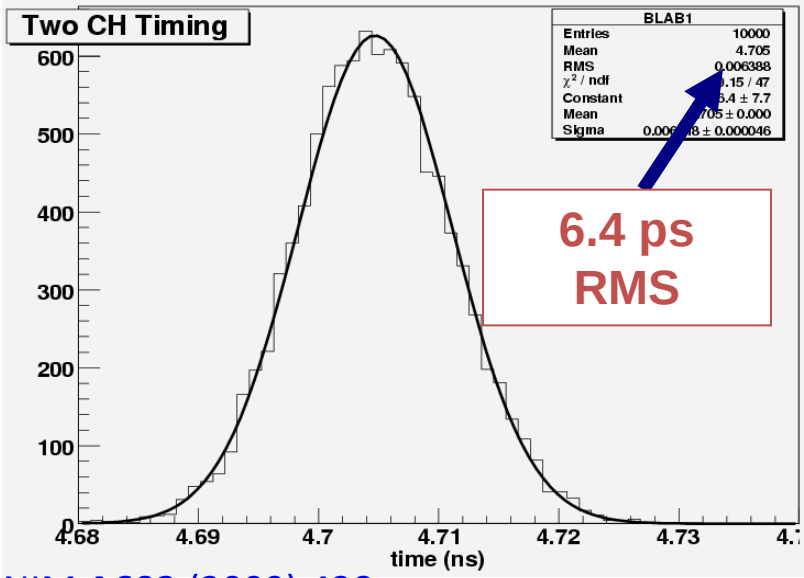
Aperture uncertainty, typical	Short term: ≤1.5 ps rms, records having duration ≤100 ms ≤800 fs rms, records having duration ≤10 μs Long term: ≤15 parts per trillion rms, records having duration ≤1 minute

Readout Electronics

- Building on experience from existing devices & readouts.
  - Readout based on waveform sampling
  - Requirements of the readout vary significantly by application

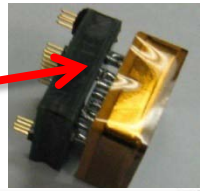


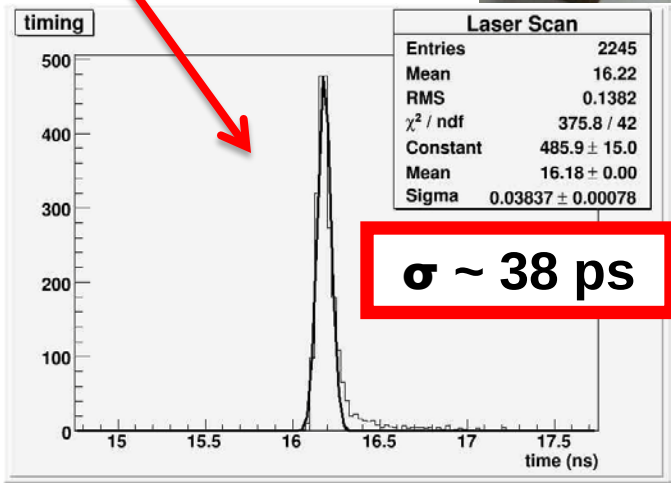


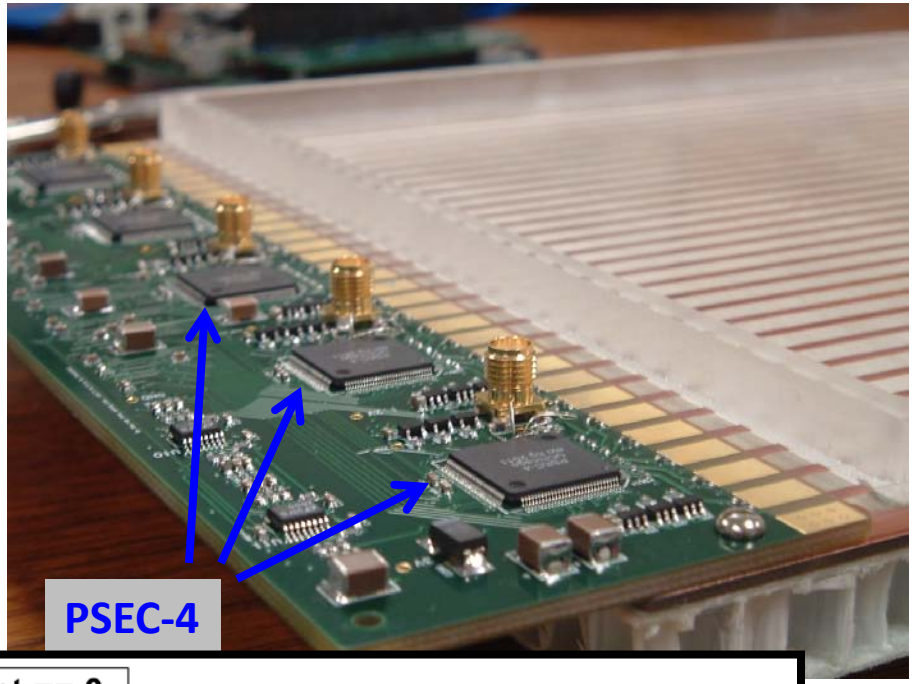
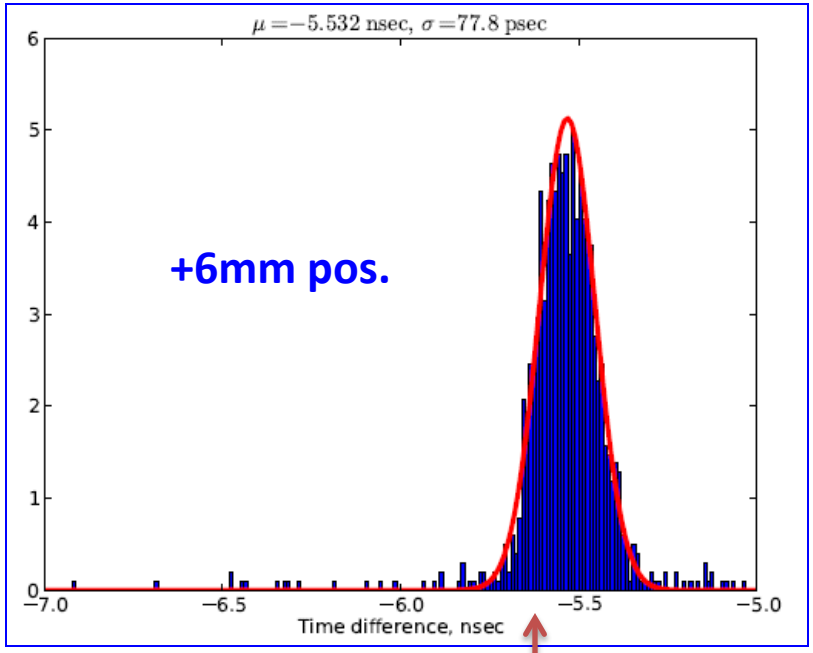
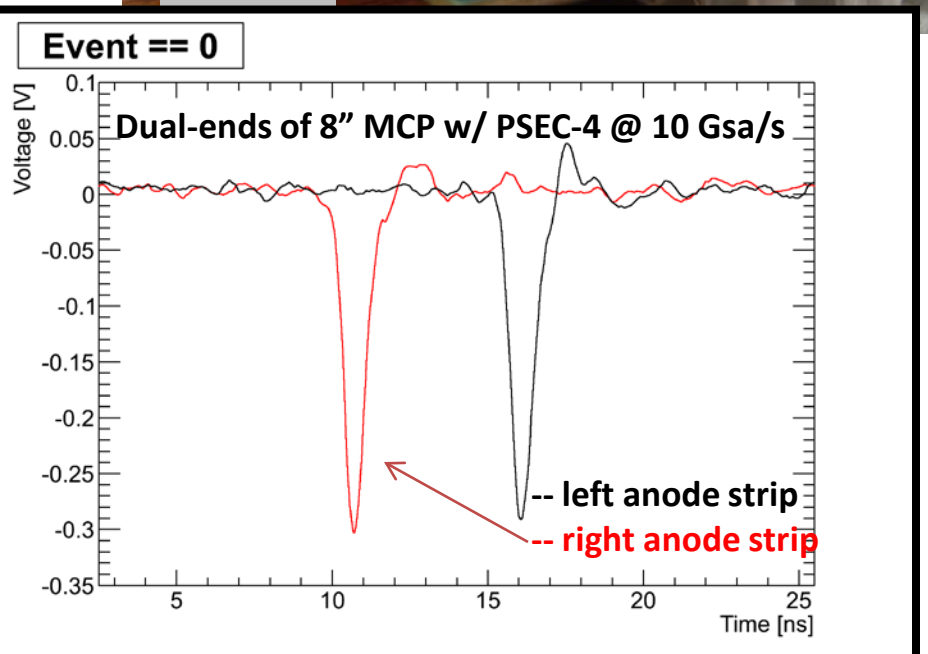
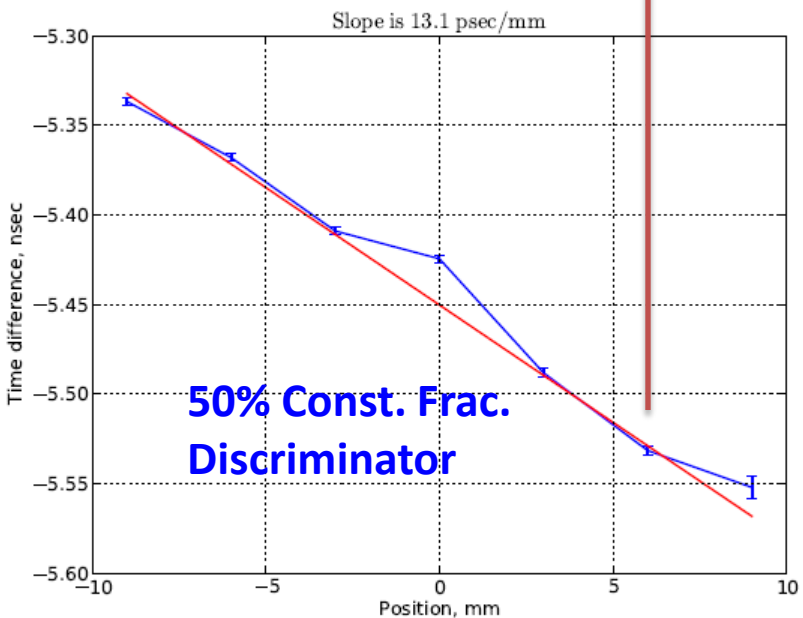


NIM **A602** (2009) 438

4x4 anode "1 inch"
MCP-PMT (HPK SL-10)





Single p.e. resolution

PSEC-4 measurements with an 8” MCP