

Questions to answer (or at least raise and discuss) in the Electronics Godparent Review

Signal Formation and Noise

1. What are the roles of the anode strip-strip gaps and MCP-anode gap in signal formation?
2. Is the current anode design optimum for our current MCP's?
3. What are the attenuation length and uniformity of our SM anode?
4. What is the expected frequency spectra of signal?
5. What is the expected frequency spectra of each of the noise sources?

Sampling Rate, AWB, Buffer Depth, Number of Channels, Readout Speed needed for various Applications

1. What are the sampling rate, AWB, buffer depth, number of channels, and readout speed needed for LBNE?
2. What are the sampling rate, AWB, buffer depth, number of channels, and readout speed needed for a CDF Run-III Upgrade?
3. What are the sampling rate, AWB, buffer depth, number of channels, and readout speed needed for a forward plane in JPARC or LHCb?
4. What are the sampling rate, AWB, buffer depth, number of channels, and readout speed needed for PET?
5. What are the sampling rate, AWB, buffer depth, number of channels, and readout speed needed for a Belle II iTOP image plane upgrade?

Wave-form Sampling ASIC Status

1. Status/Performance of PSEC2 performance?
2. Status of PSEC3?
3. Status of CHAMP?
4. Other designs or plans for follow-up ASICs?
5. What is the expected cost per channel for the LBNE application?

Test Setup Status

1. Status of PSEC2 testing and flip-chip bonding?
2. Status of PSEC3 test boards and flip-chip bonding?
3. Status of CHAMP test boards?
4. Plans for anode tests using MCP signals
5. Plans for 8" tile/SM-tray tests

Analog and Digital Card Status

1. What is the ABW of matching transmission-lines to ASICs on the analog card?
2. What is the Analog card status?
3. What is the Digital card status?
4. What is the expected channel-to-channel and SM-to-SM jitter for the current plans for clock cleaning and distribution?

Tray Status

1. What is the current baseline design for tray construction?
2. What are the input and output interfaces?
3. What are the component costs?
4. What is the plan and schedule for constructing trays?
5. What are the plans for testing complete trays?

DAQ and Data Analysis

1. What is the status of firmware for PSEC2 and PSEC3?
2. What is the status of firmware for the CHAMP?
3. Where are there test setups for ASICs, and what manpower?
4. What are the performance goals of the DAQ?
- 5.

Expected Performance

1. What is the expected MCP gain for single photo-electrons and for 50 pe's?
- 2.
- 3.
- 4.
- 5.
- 6.

Next Steps

- 1.
- 2.
- 3.
- 4.
- 5.