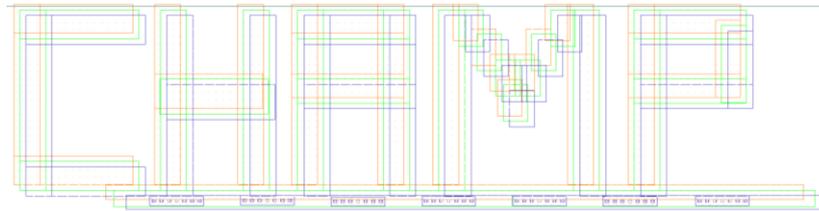


The CHAMP ASIC and ASIC Options



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LAPPD Electronics Godparent Review

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A bit of context...

- Hawaii (Gary) has a lot of ASIC experience with TSMC 0.25 μm .
 - As of beginning of last year, no direct experience with IBM 0.13 μm .
- Most waveform sampling/digitizing ASICs are in larger processes ($\geq 0.25 \mu\text{m}$) ...

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

➔ **Success of PSEC3: proof-of-concept of moving toward smaller feature sizes.**

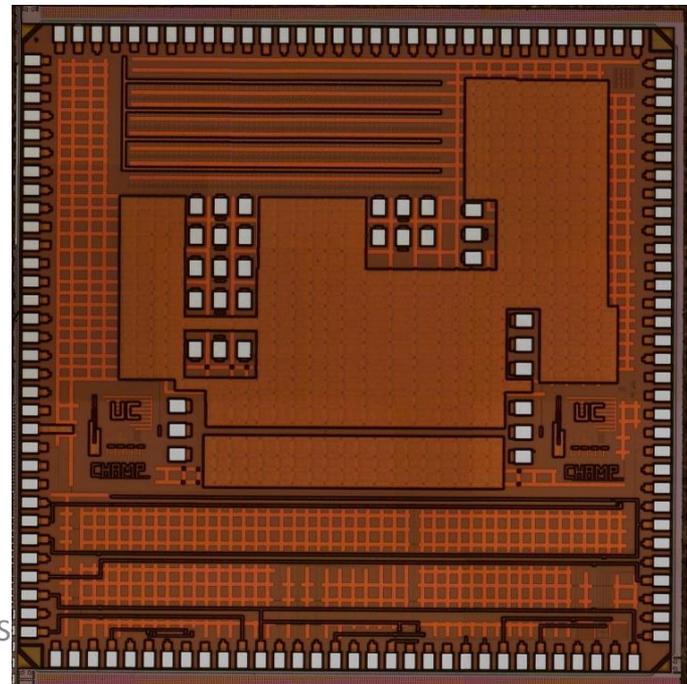
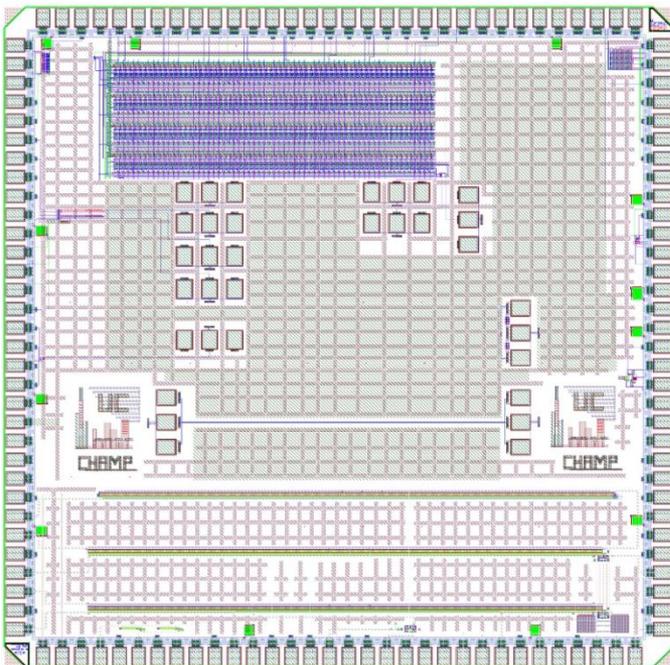
- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

CHAMP

- Chicago-Hawaii ASIC, Multi-Purpose:
 - First experience for Hawaii...
 - ...in the IBM 0.13 μm process for all of us.
 - ...in ASIC design for a few of us.
 - Hawaii submission was primarily to:
 - Characterize structures that may be useful on future ASICs.
 - Gain a feel for the IBM process.
 - Provide some training for new ASIC designers.
 - On Chicago side:
 - Primarily independent versions of structures that were similar or identical to PSEC3 for planned characterization & independent debugging.

CHAMP

- Submitted as part of CERN MPW in May 2010.
 - First experience submitting through CERN:
 - Excellent future resource, much technical expertise.
- First die received from CERN Feb. 14th 2011.
 - ~9 month turnaround (PSEC3 submitted in the mean time.)
 - ~200 die: about same cost as 40 through MOSIS



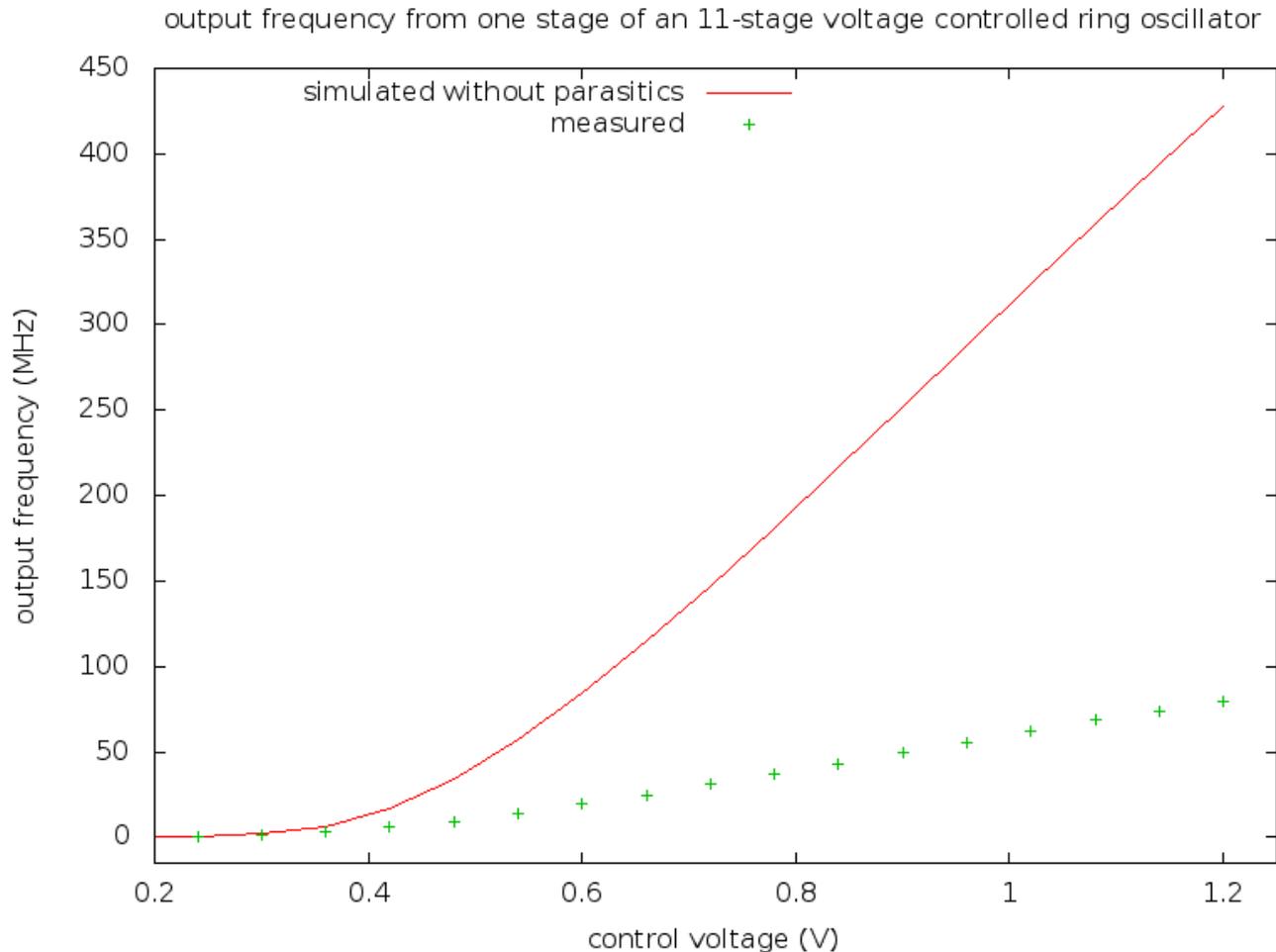
Hawaii Structures on CHAMP

- D flip-flops
- Voltage controlled delay line (VCDL) (x2)
- Voltage controlled ring oscillator (VCRO)
- Digital-to-analog converter (DAC)
- Waveform sampler arrays (WFS) (x4)
- Analog storage cells with built-in comparator
- LVDS receiver
- Charge sensitive amplifier (CSA)

Chicago Structures on CHAMP

- VCDLs w/ delay locked loops (DLLs)
 - “Slow” (18 GHz)
 - “Fast” (25 GHz)
- Independent DLL structure
- VCROs + counters
 - “Slow” (3 GHz)
 - “Fast” (4 GHz)

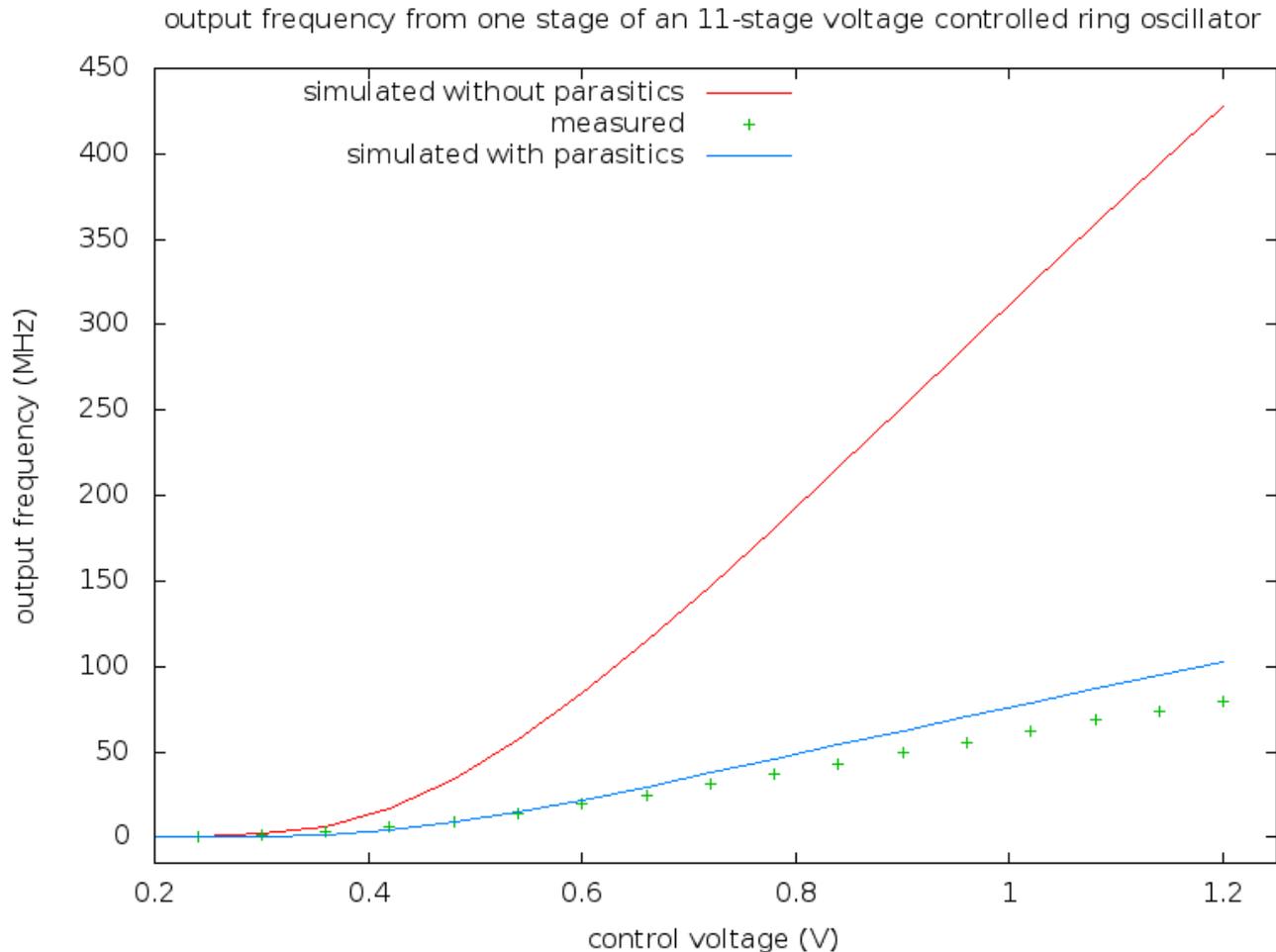
CHAMP Results (Hawaii) - VCRO



- Initial data/simulation* agreement was very bad...

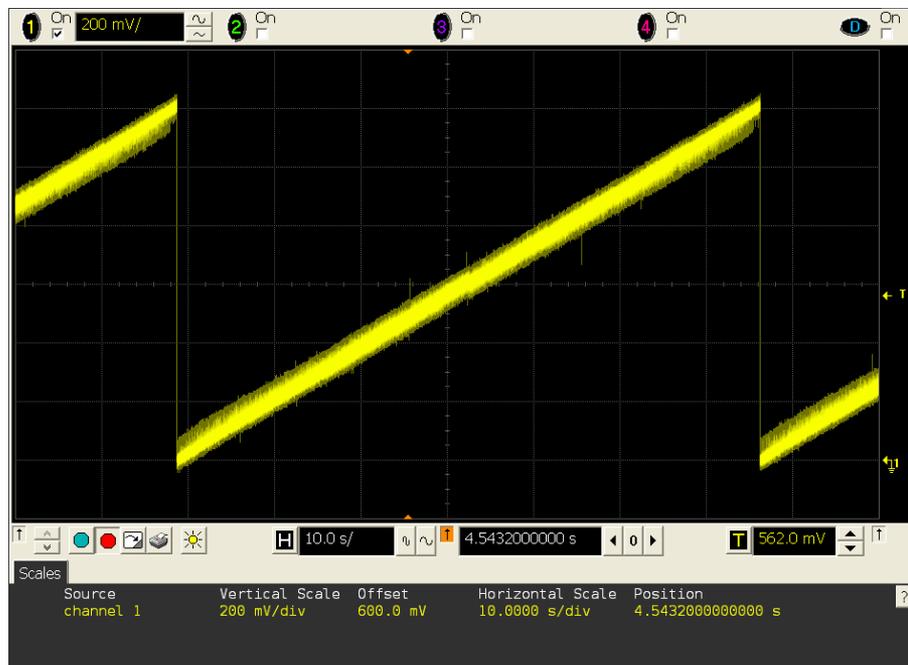
*Parasitic extractions not working in Hawaii during CHAMP design.

CHAMP Results (Hawaii) - VCRO



- A lesson learned the hard way → simulation without parasitics is almost useless for quantitative predictions... fixed now.

CHAMP Results (Hawaii) - DAC

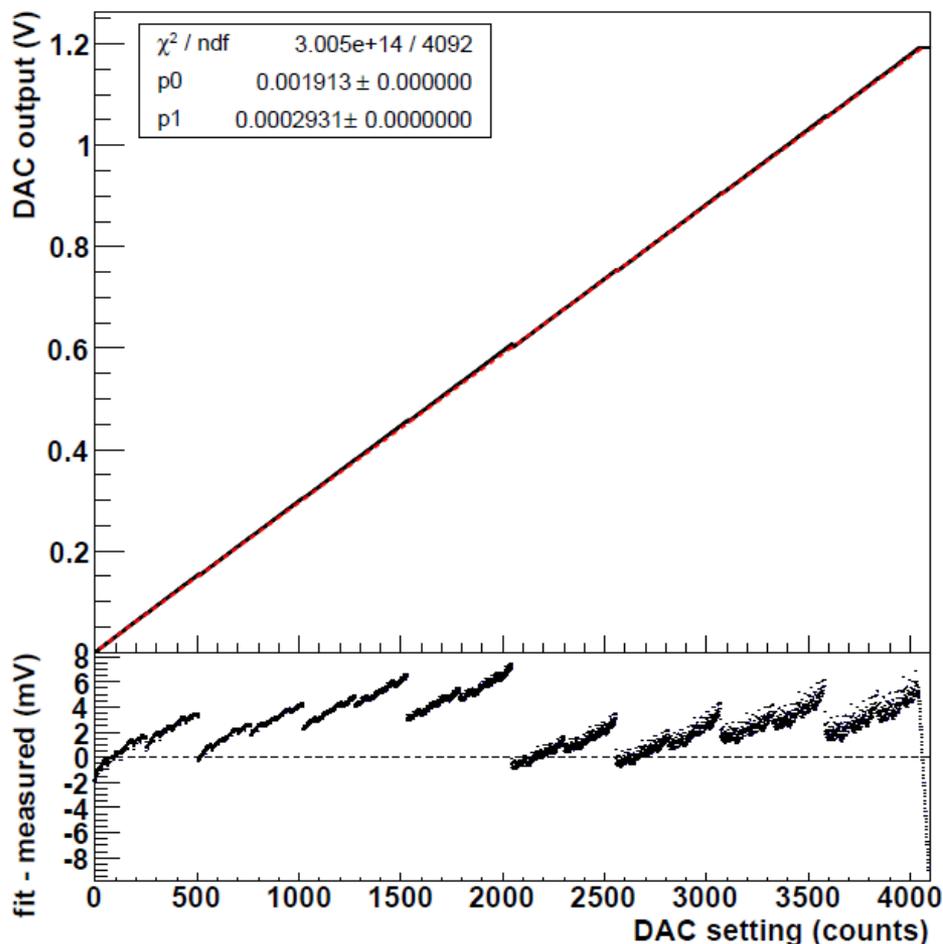


Prototype for future submissions

- Moving DAC internal to ASIC can save on:
 - Pins needed for external biasing.
 - Board real estate previously used by external DACs.

- CHAMP DAC ramping up from minimum to maximum voltage.

CHAMP Results (Hawaii) - DAC



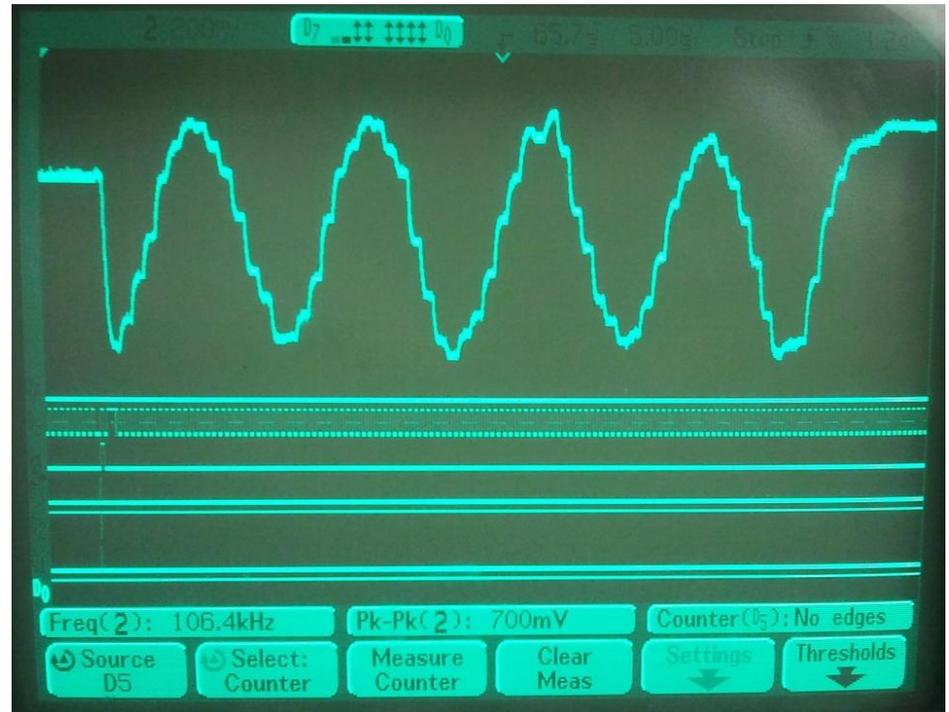
DAC Performance:

- Linear to within a few mV.
- No significant gaps in voltage coverage.
- ***Very usable in future submissions.***

CHAMP Results (Hawaii) - WFS

Waveform Sampler

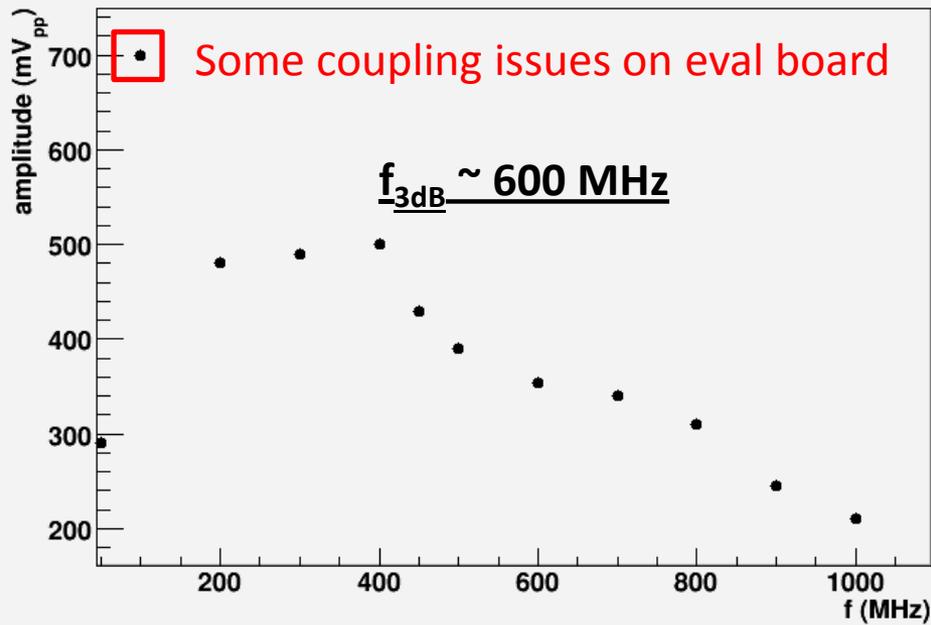
- Four sampling arrays:
 - Different combinations of analog switches and capacitors.
 - No on-chip ADC, analog voltage out.
 - Sampling rate ~ 1.5 GSa/s.
- Primarily to study bandwidth.



Analog voltage out w/ 100 MHz sine wave input.

CHAMP Results (Hawaii) - WFS

Preliminary Waveform Sampler CH3 Rolloff



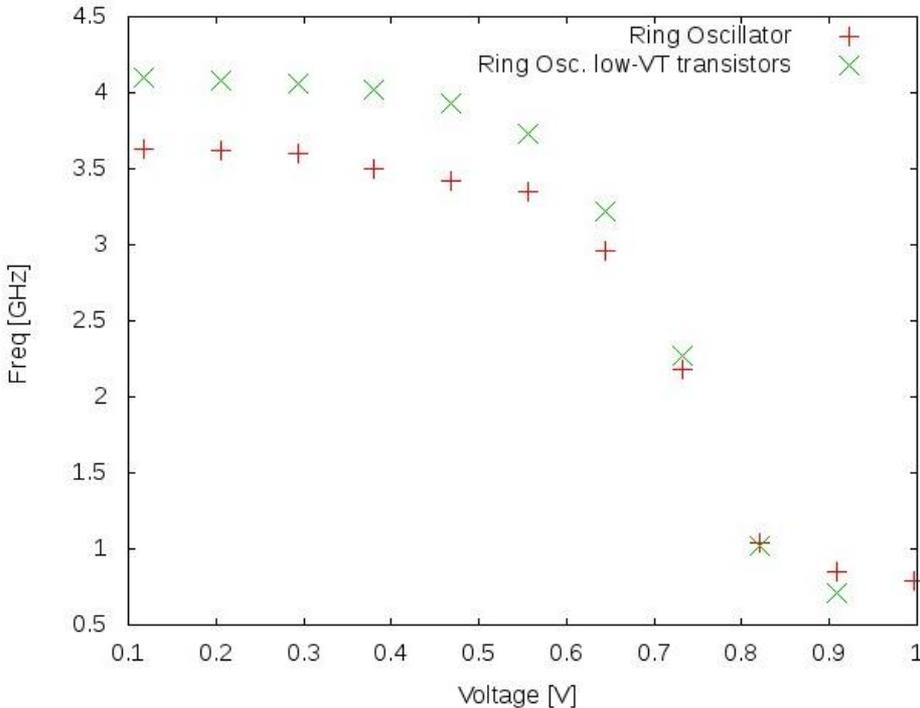
Measured response of sampling array

Analog voltage out w/ 100 MHz sine wave input.

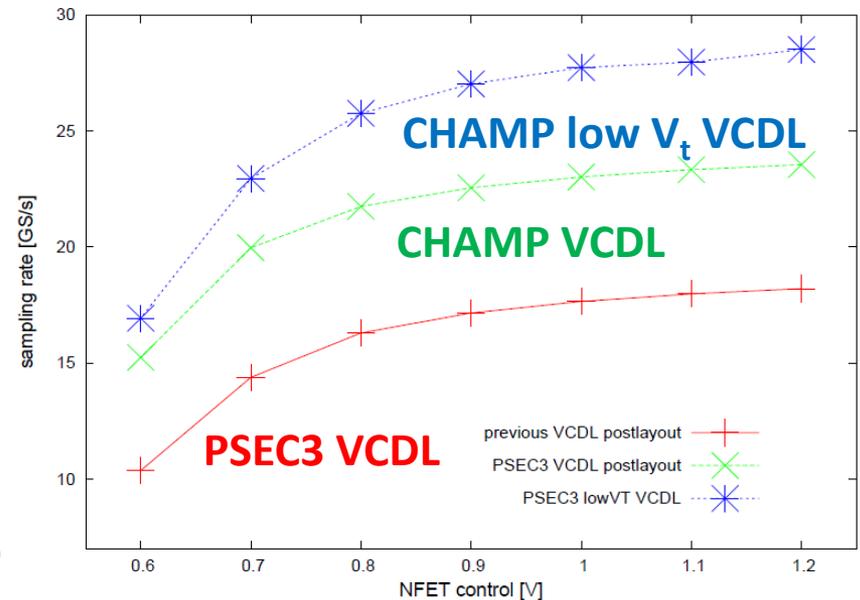
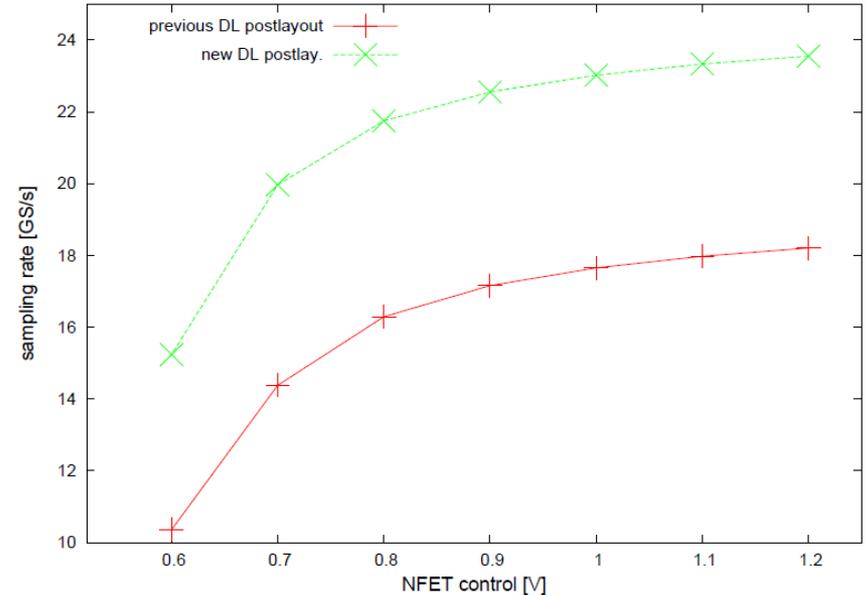
➔ Initial results indicate bandwidth comparable to PSEC3. Studies are ongoing.

CHAMP Results (Chicago)

Ring oscillator frequency measurements



VCDL post-layout simulation results



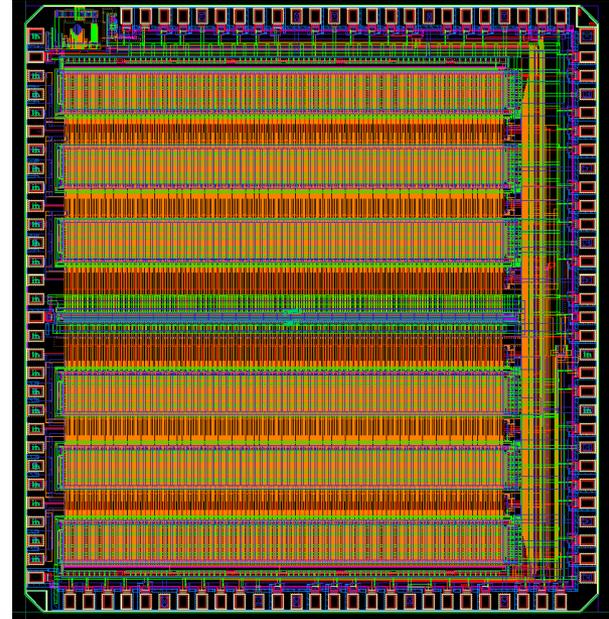
- Many structures tested on PSEC3 already...
 - But faster versions on CHAMP, including low V_t transistors

CHAMP Lessons Learned

- Characterization still ongoing, but have already learned a lot:
- Submission through CERN MPW:
 - Provided significant technical expertise & assistance.
 - This particular submission had long delay...
 - Anecdotal... just bad luck?
 - ...but also got many more chips for same price.
 - Pricing details depend on specific MPW run.
- Hawaii:
 - Experience w/ ASIC design, IBM 0.13 μm .
 - Several new people introduced to ASIC design.
 - Parasitics are vital! Now working well in Hawaii.
- Chicago:
 - Prototyped some of fastest structures yet, including low V_t versions.
- Both:
 - Many structures usable for future submissions.

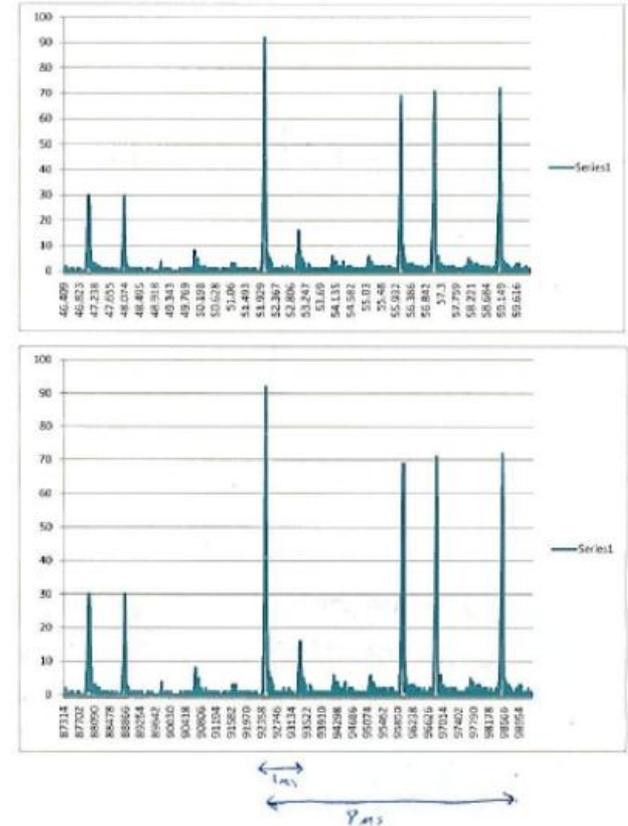
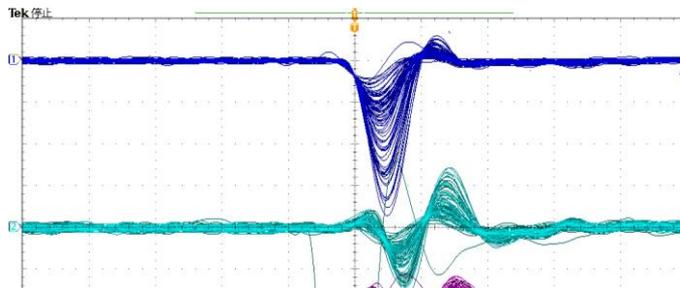
The “AS” in ASIC

- PSEC3 is quite successful!
 - ➔ Anticipate PSEC4 will be even more so.
- We do not expect PSEC4 to fail...
 - ...but we also recognize it can not be “application specific” for every application:
 - Designed to handle fast pulses (MCPs)
 - Sampling rate capability > 10GSa/s
 - Analog bandwidth > 1 GHz (challenge!)
 - Relatively short buffer size
 - Medium event-rate capability (~100 KHz)



Example “AS” requirements

- Large buffer depths and/or trigger latencies.
- On-chip amplification for single p.e. detection.



➔ Strategy: leverage existing ASIC designs as needed.

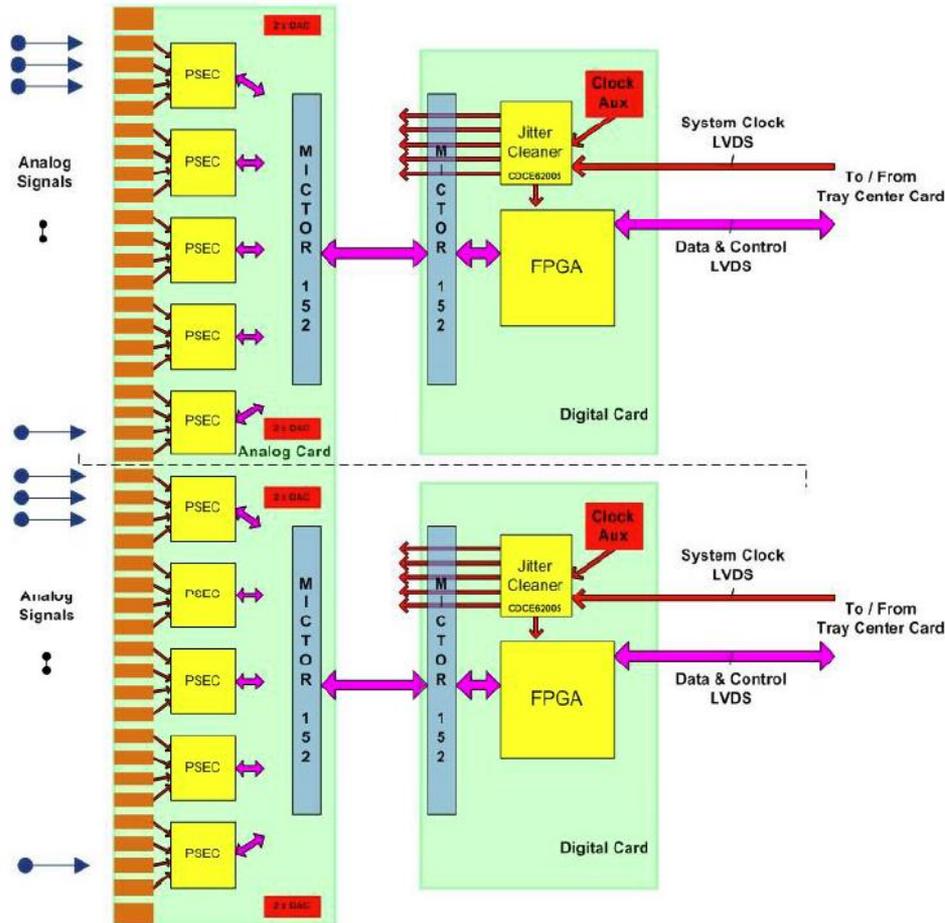
Snapshot of fabricated ASICs (Hawaii)

All in TSMC 0.25um

ASIC	# Ch.	Sampling (GSa/s)	ABW (GHz)	# Samples	# Store cells/chan.	Remarks
LAB3	8+1	0.5-3.2	0.8	256+4	same	
BLAB1	1	0.5-6	0.2	64K	same	
BLAB2,3	8	0.5-4	0.3	2*64	32K	- 2stage x-fer - Amplification
IRS, IRS2	8	0.5-3.3	1/?	2*64	32K	- 2stage x-fer
TARGET	16	0.5-2.5	0.2	4K	same	
TARGET2,3	16	0.5-2.0	0.4/1	2*32	16K	- 2stage x-fer - Amplification on TARGET2
STURM	8	10-20	~2	4*8	same	
STURM2	8+1	1-200	~3	4*8	same	
LARC	64	0.5-3.5	0.5	1K	same	

- Variety of ASICs with varying bandwidths, sampling depths, with and without amplification.

Hardware w/ Alternative ASICs



- Baseline hardware continues to be based on PSEC ASICs.
- In the event of unforeseen problems (or for alternative applications):
 - New analog cards could be designed to accommodate alternate ASICs.
 - In short term, such designs would delay baseline effort.

*Details of system development in Mircea's talk next.