Alternative ASIC Options

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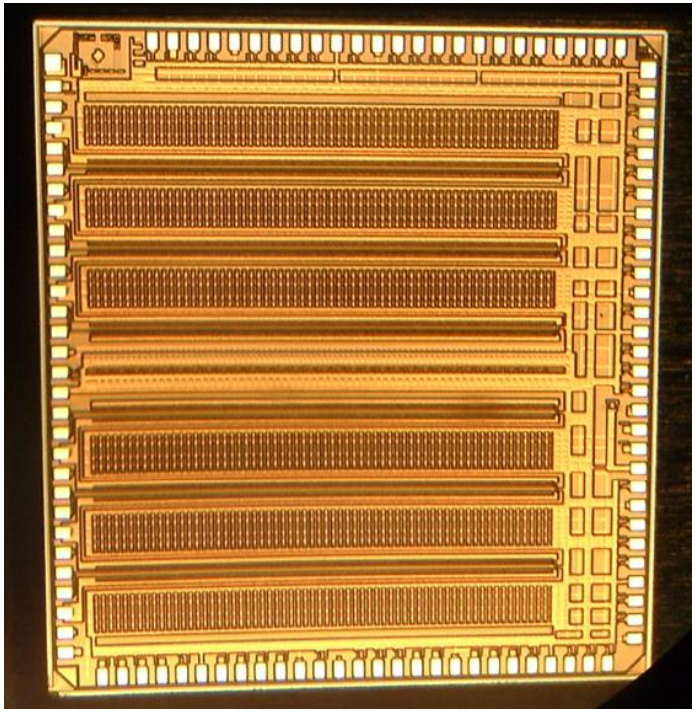
PSEC-4 Features

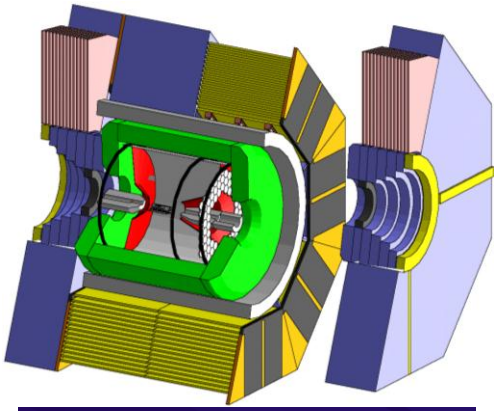
- **Specifications:**
  - **Multi-channel: 6 channels**
  - **Excellent bandwidth: > 1.5 GHz**
  - **Fast sampling: > 10 GSa/s**
  - **Low noise: < 1 mV_{RMS}**
  - **Dead time:**
    - **~700 ns (conversion) + (readout)**
    - **Event rate: ~100s of kHz**
  - **Buffer depth: 256 samples**
    - **25.6 ns at 10 GSa/s**

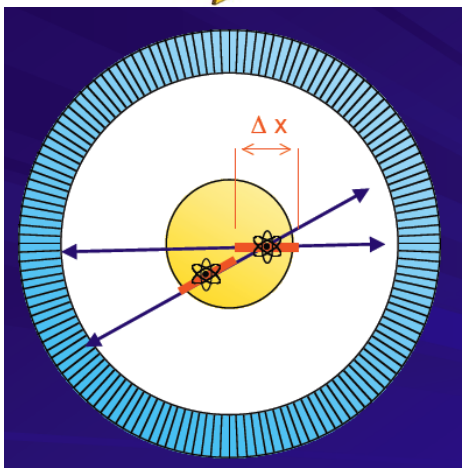


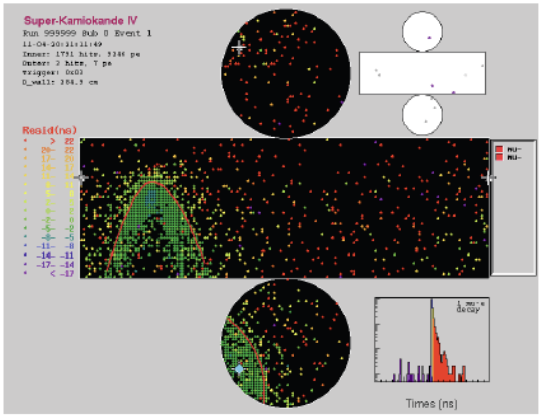
- **Excellent performance demonstrated as a very fast, high-bandwidth sampler.**
  - **Some applications have different requirements…**

Application Specific Requirements

- Deep buffering
  - Long trigger latencies create need for very deep analog storage buffer.
  - Example: Belle II subdetectors must accommodate ~5 μs of trigger latency.
- Fast readout, low dead-time
  - High event rates require fast digitization, multi-hit buffering, or both.
  - Example: PET, ~MHz level hit rates.
  - Example: "Triggerless" acquisition, all hits digitized, trigger formed in software.







Selected Hawaii ASICs

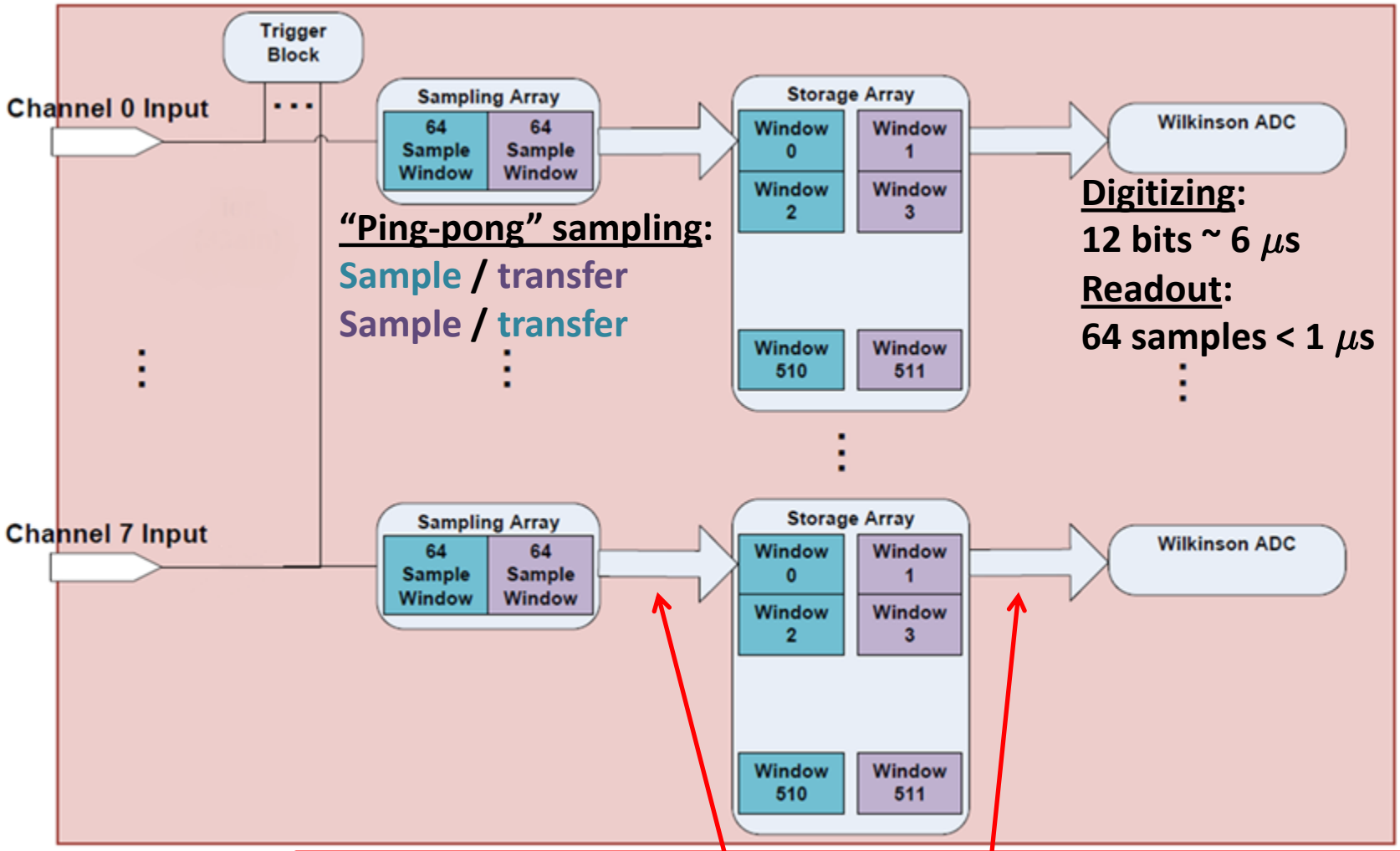
ASIC	# Ch,	Sampling (GSa/s)	ABW (GHz)	Sample Cells	Storage Cells	Remarks
LAB3	8+1	0.5-3.2	0.8	256+4	256+4	
BLAB1	1	0.5-6	0.2	64K	**64K**	
BLAB2	**16**	0.5-4	0.2	3K	3K	**- On-chip amp**
IRS2	8	0.5-3.3	>1	2*64	32K	- 2stage x-fer
➔IRS3B	8	0.5-4.0	~1	2*128	32K	- 3stage x-fer
TARGET	**16**	0.5-2.5	0.2	4K	4K	
TARGET4	**16**	0.5-1.5	~0.5	2*32	16K	- 2stage x-fer
➔TARGET5	**16**	0.4-1.2	~0.5	2*32	16K	- 2stage x-fer
STURM	8	**10-20**	**~2**	4*8	4*8	
STURM2	8+1	**1-200**	**~3**	4*8	4*8	
LARC	64	0.5-3.5	0.5	1K	4*8	
RITC	3	0.2-0.6	>1	32	32	- 3-bit streaming output
➔RITC2	3	0.2-2.6	>1	32	32	

TSMC 0.25um

IBM 0.13um

➔ Variety of bandwidths, depths, performance tradeoffs.

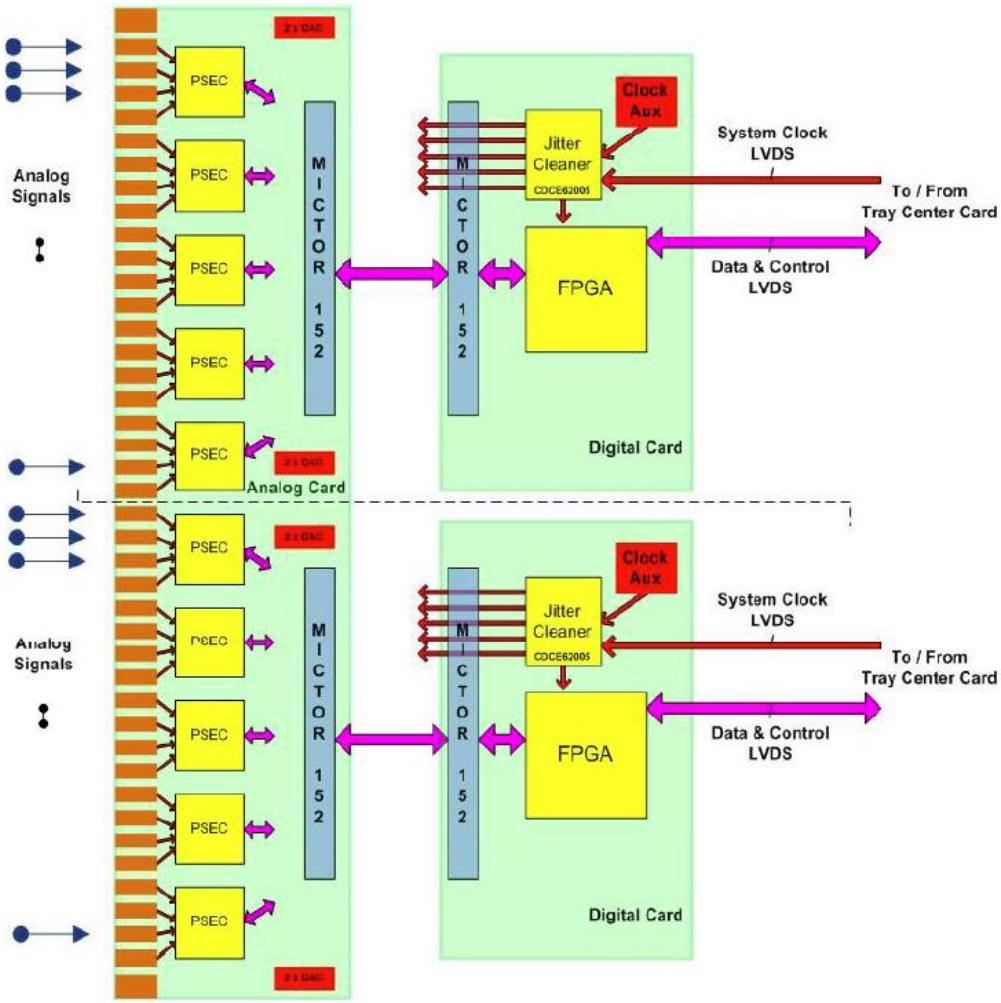
Multi-stage transfer architecture



Analog storage and digitize operations can happen in parallel.

➔ **Designed for deep buffering, parallel digitization & sampling.**

Front-end w/ Alternative ASICs



- Baseline hardware is designed around PSEC-4.
- During design of digital cards, effort was made to make digital card compatible with a possible IRS2 analog card.
  - Other UH ASICs are almost certainly possible as well.
- Cards could be designed, fabbed as need arises.

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

➔ **Success of PSEC3: proof-of-concept of moving toward smaller feature sizes.**

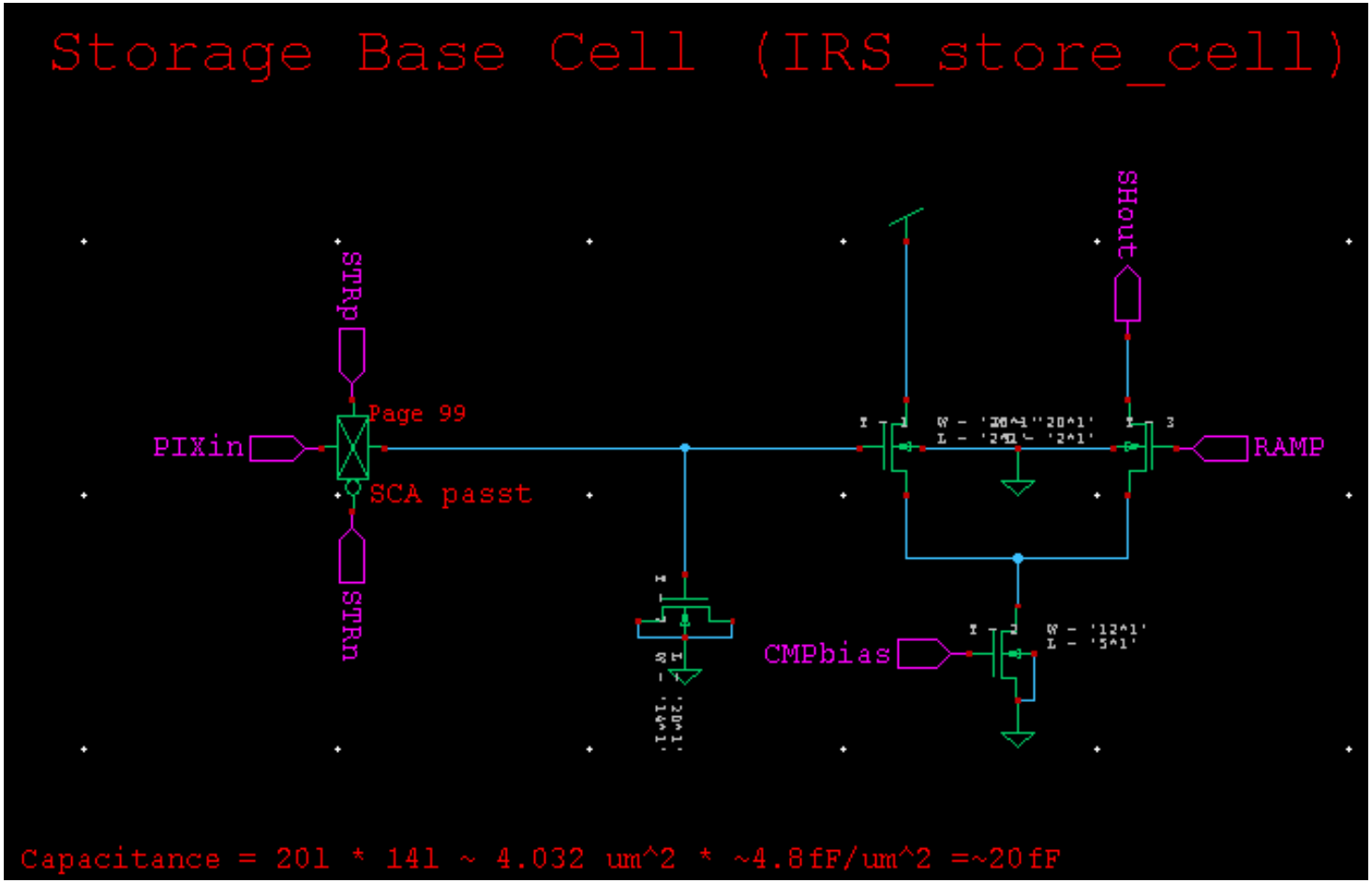
- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

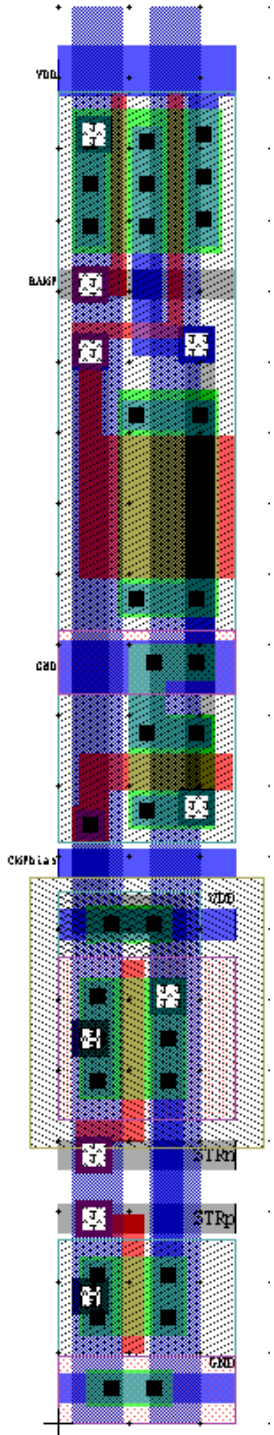
SAM/SAMLONG Specifications

NAME	SAM	SAMLONG (measured)	Unit
Power Consumption	300	160-250	mW
Sampling Freq. Range	<1to 2.5 (3.2)	0.4 to 3.2GS/s	GS/s
Analog Bandwidth	250-300 (450MHz)	400	MHz
Read Out time for a 16 cell event (2 gains 1- cells)	< 1.5	<2	µs
Fixed Pattern noise	0.4	0.35	mV rms
Total noise (constant with frequency)	0.65 (0.5mV if FPN cancelled)	0.65 (0.55mV if FPN removed)	mV rms
Maximum signal (limited by ADC range)	2 (4)	2V (ADC limited)	V
Dynamic Range	>11.6 (12.6)	>11.6	bits
Crosstalk	<3	<3	per mil
Relative non linearity	< 1	<3	%
Sampling Jitter	<15	<18	ps rms

**From Eric Delagnes's talk @ January Clermont workshop.

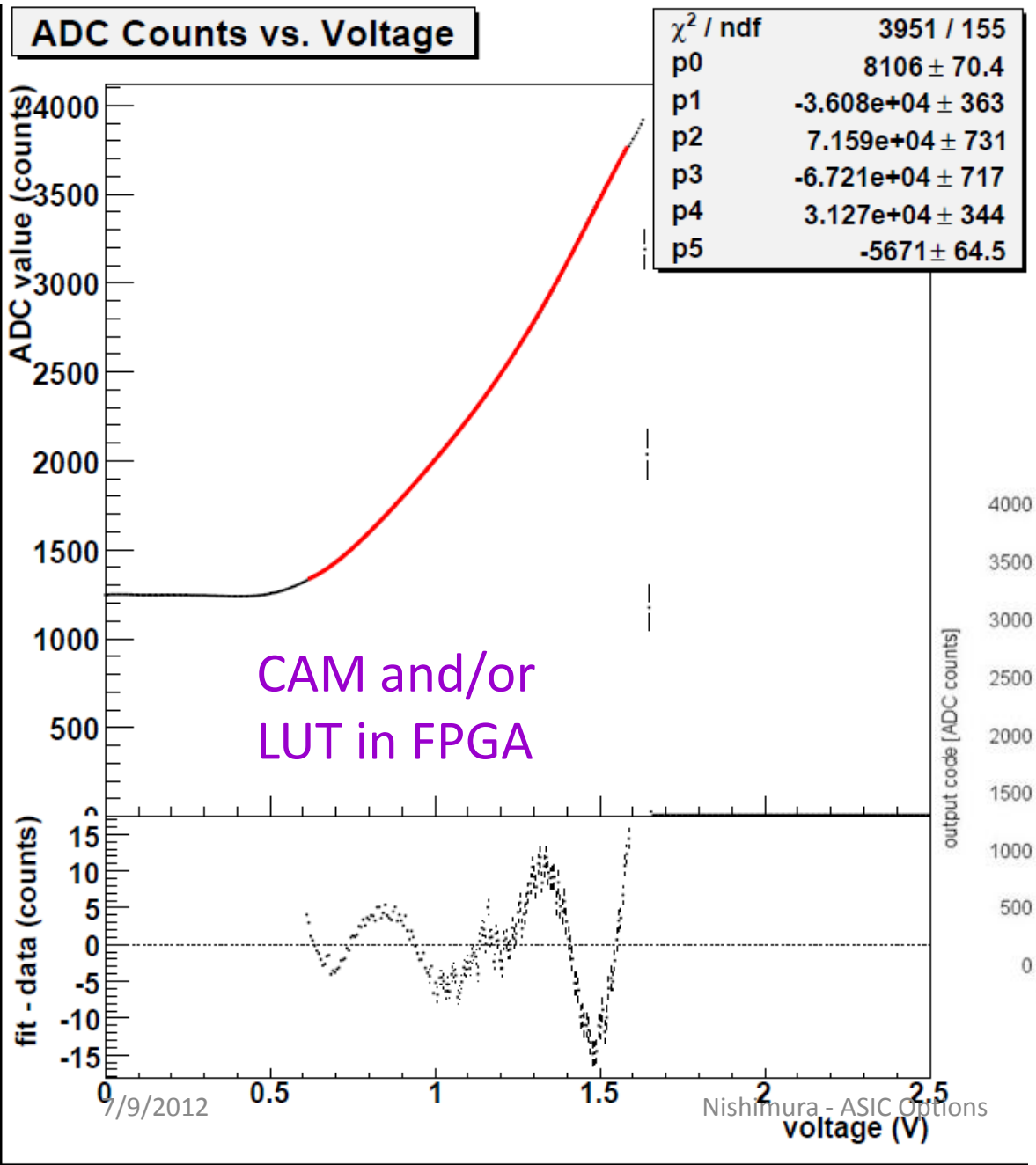
Storage Cell - compact



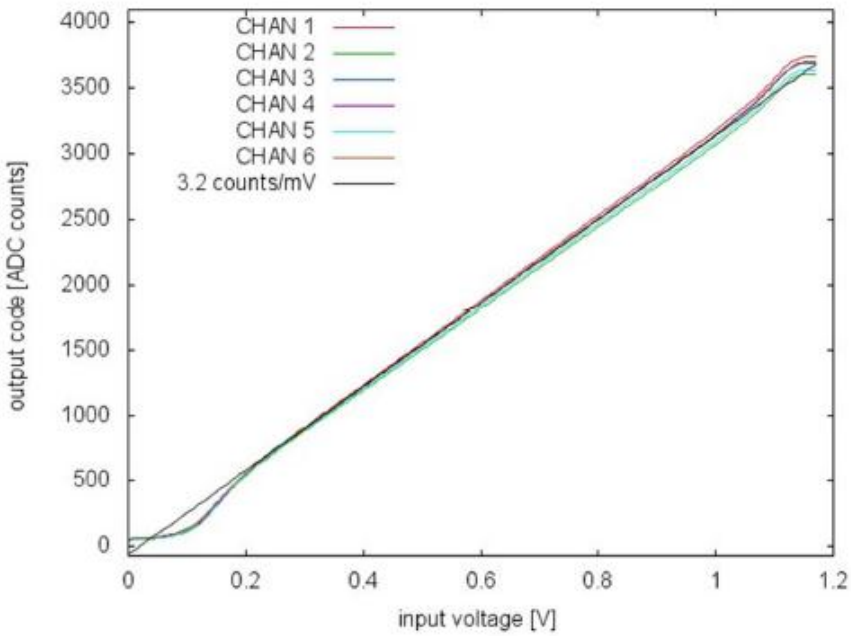


- Diff. Pair as comparator
  - Density ~ 25k storage cells/mm^2 (0.25um)

Linearity Calibration



➔ Compactness of comparator has its drawbacks…

(Left) IRS2 linearity

(Below) PSEC-4 linearity