LAPPD Electronics

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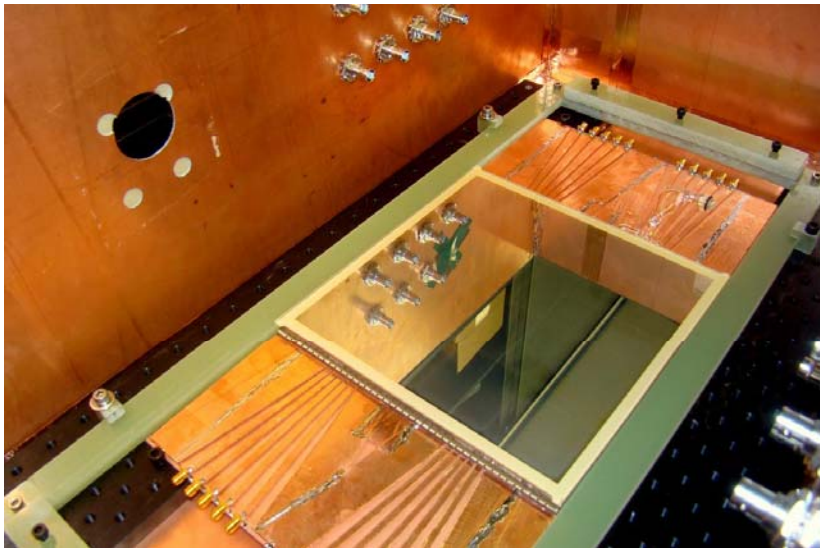
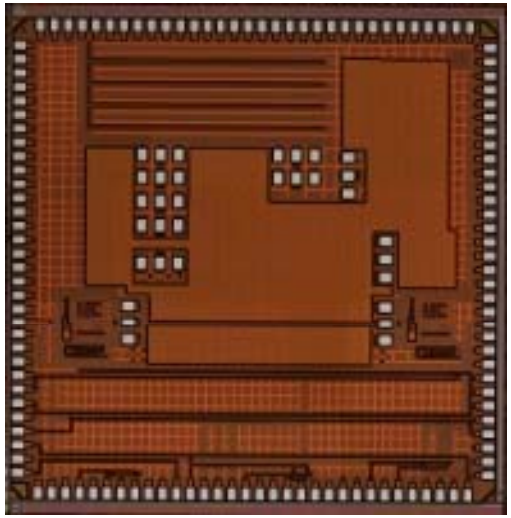
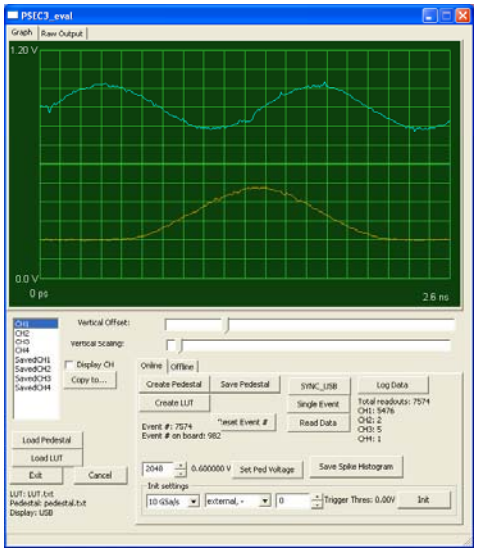
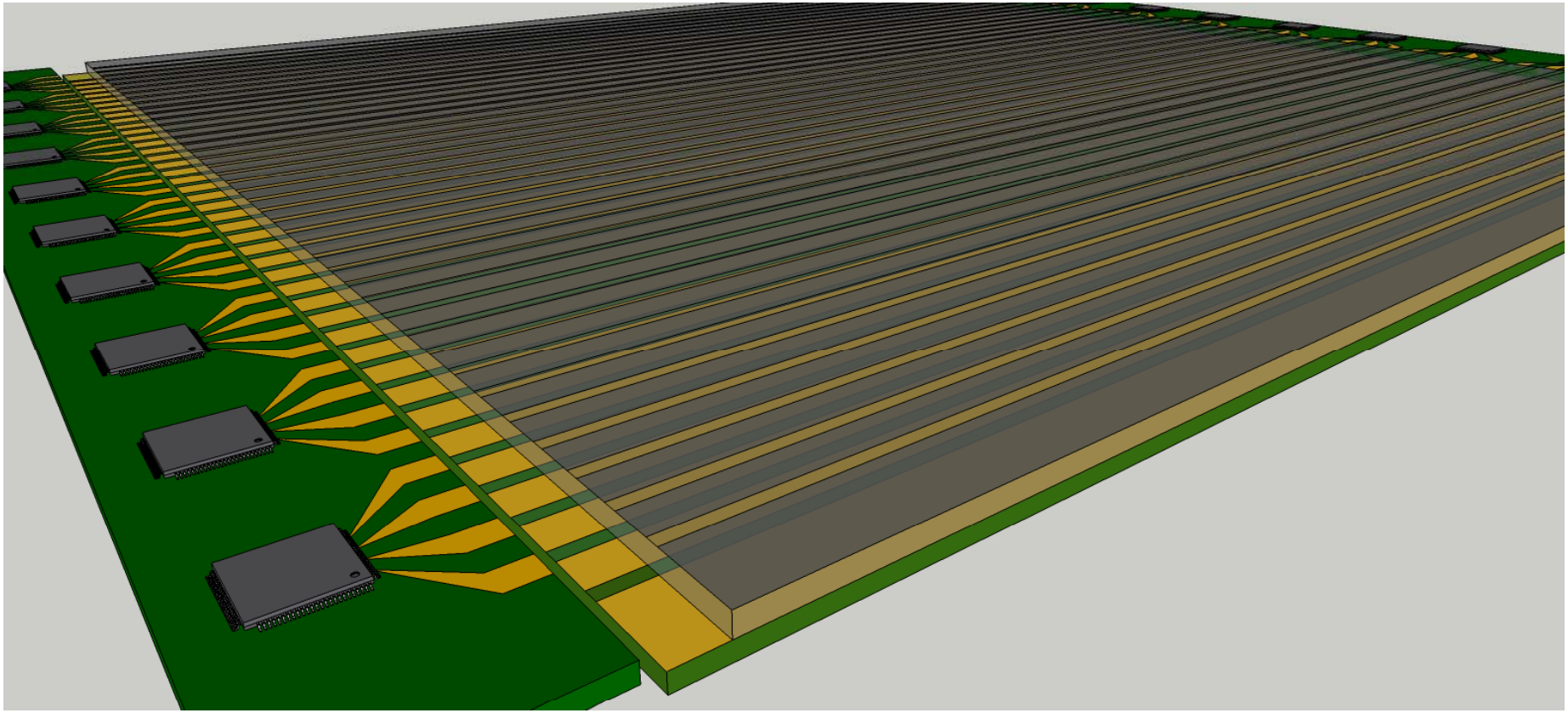
25-MAY-2011 == DOE Review at ANL





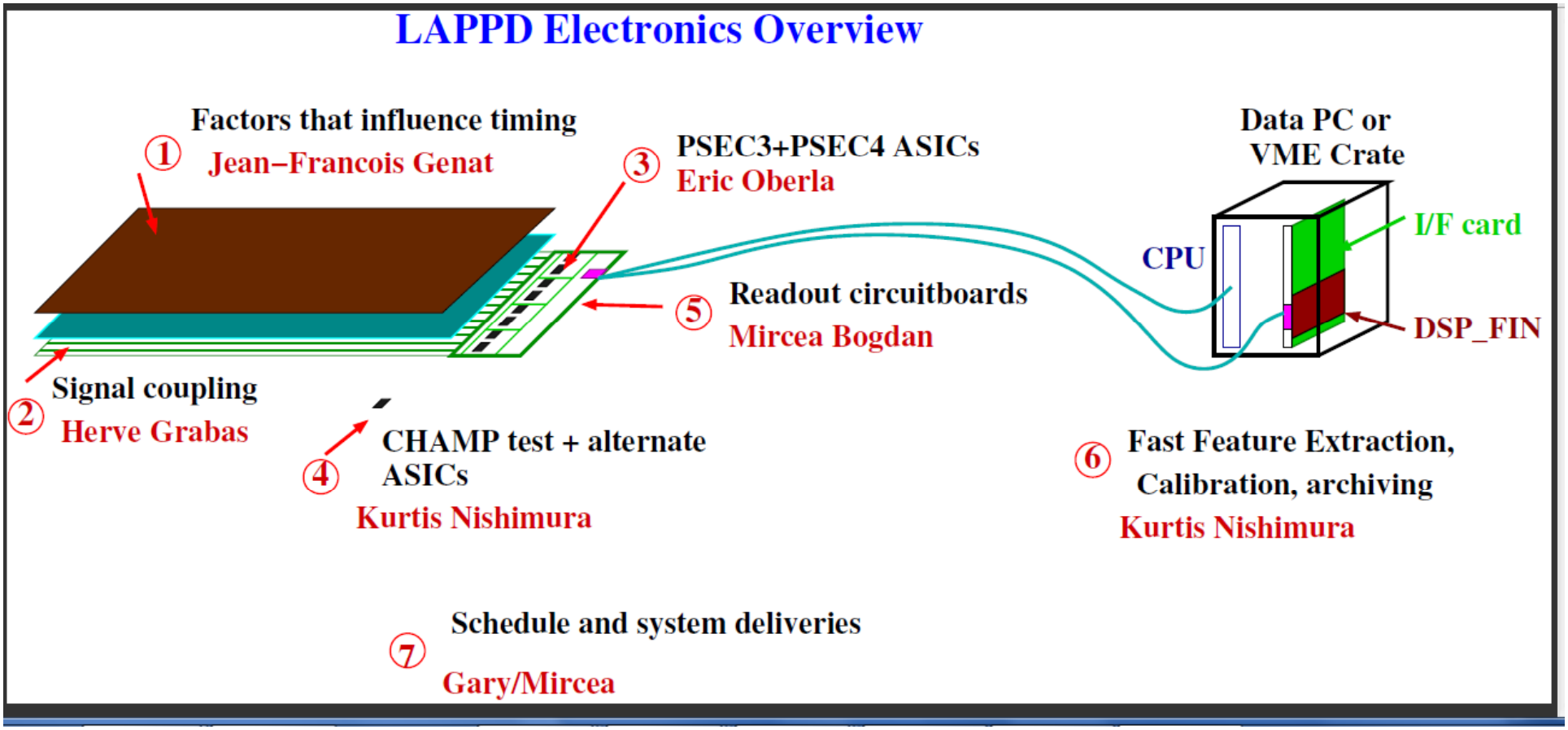


An ideal (integrated) Photodetector



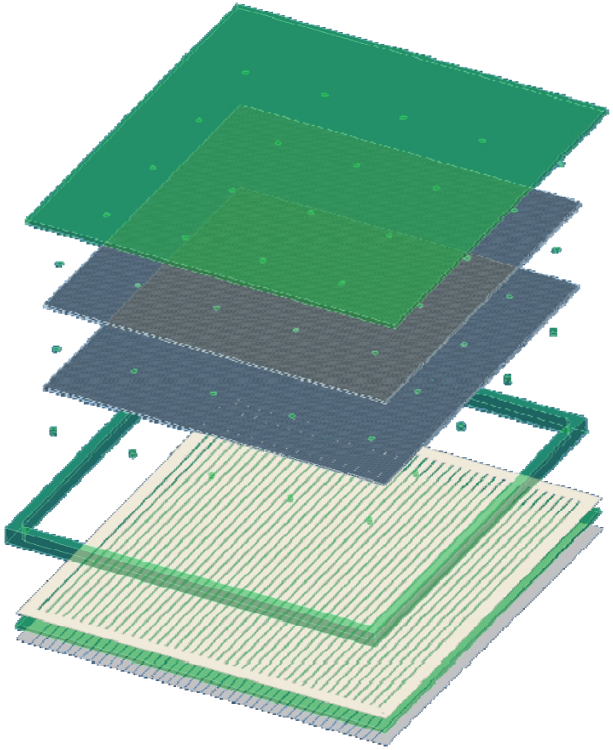
- DC power in, fiber optic out
- Integrated photon → electrons → T,Q → data out

From godparent review (last Friday)



- Addressing all aspects needed to realize integrated PD goal
- Overview only – much fundamental work underlying

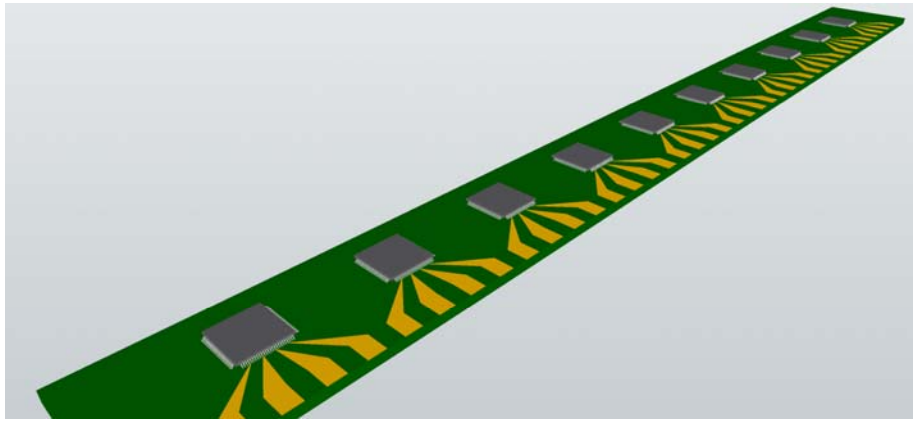
Large Area MCPs



Large Area MCP structure:

- Custom photo-cathode
- 2-plate chevron (high gain)
- Transmission line 2D readout

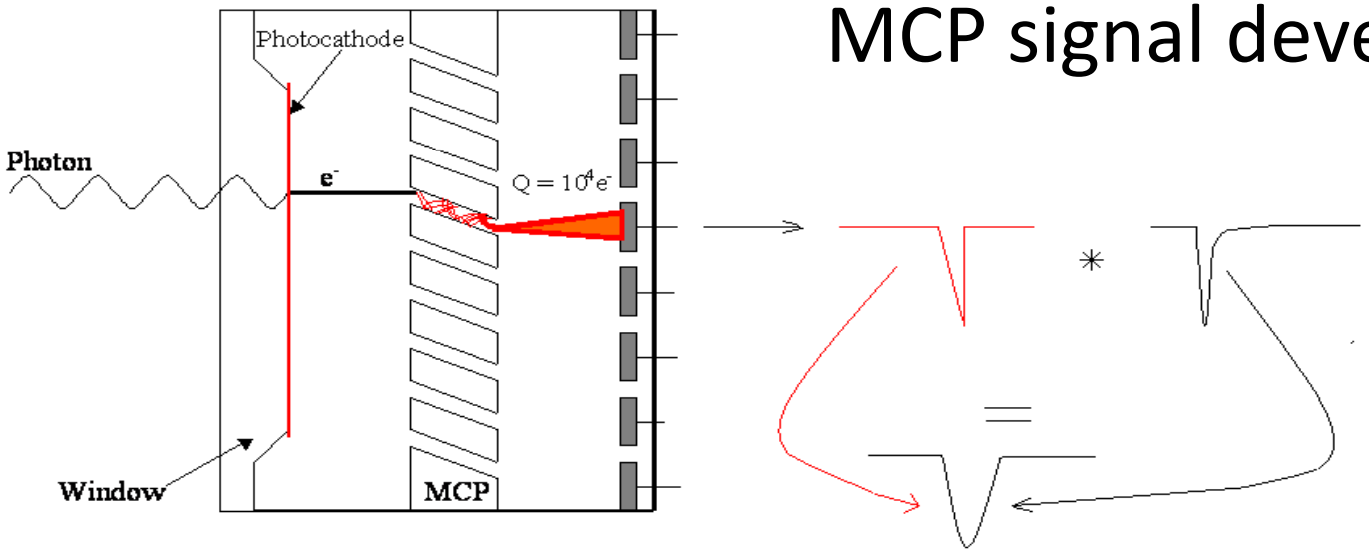
(limit the number of electronics channels)



Electronics:

- **GSa/s Waveform Sampling + Signal processing**

MCP signal development



MCP signal rising edge: qE = ma $tr = l\sqrt{2m/qV}$

l = 1mm, E=100V/mm, tr=250ps

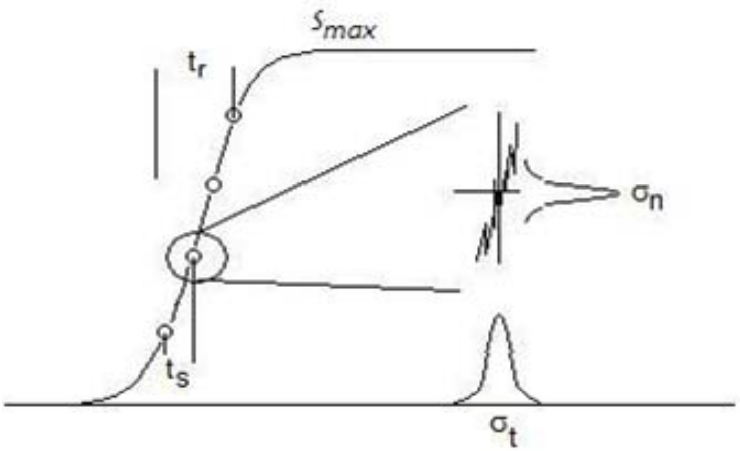
- First gap: 10ps
- Assume 2-stage pores TTS of 20ps
- Anode gap: 10ps
- Noise: 20ps

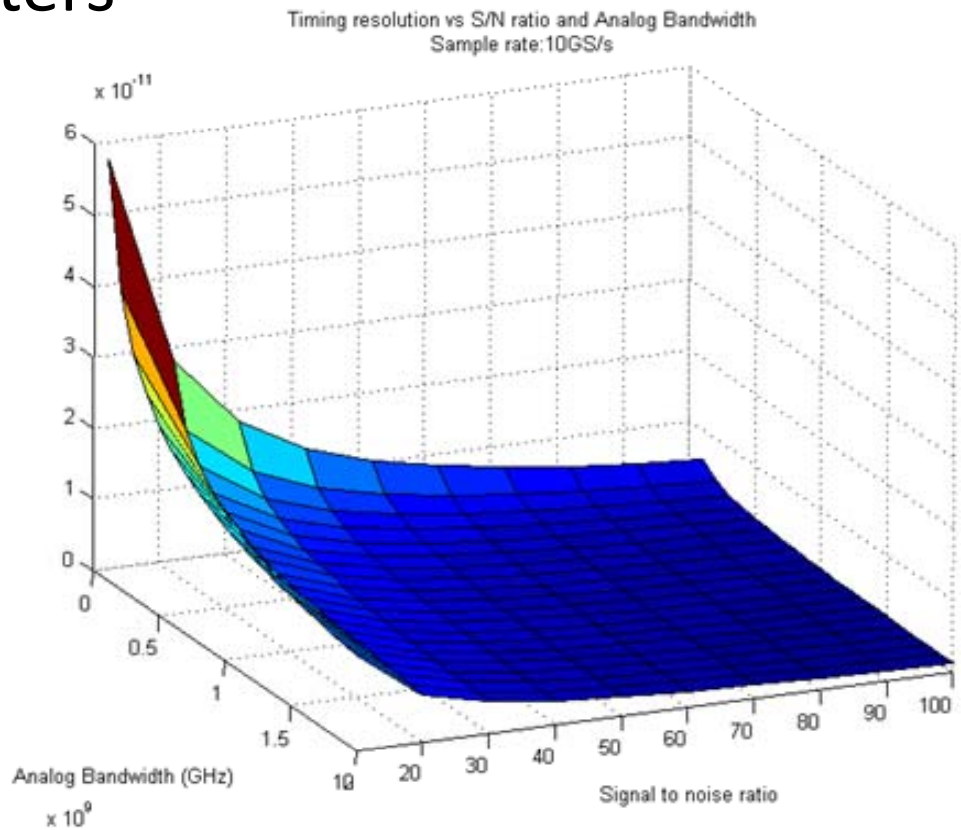
Total is 32ps

(Measured Burle-Photonis 2'' x 2'' is 30ps)

Understanding what matters

Transit Time
Noise$_{detector}$
Rise time
Gain (Signal/noise)





Electronics:

Noise$_{elec}$
Sample rate
Analog bandwidth

$$SN = S_{max}/\sigma_n \qquad \sigma_{t,n} = \frac{\sigma_n}{\sqrt{n}}$$

$$\sigma_{t,n} = \frac{\sqrt{t_r t_s}}{SN} = \frac{1}{SN}\sqrt{\frac{0.35 t_s}{abw}}$$

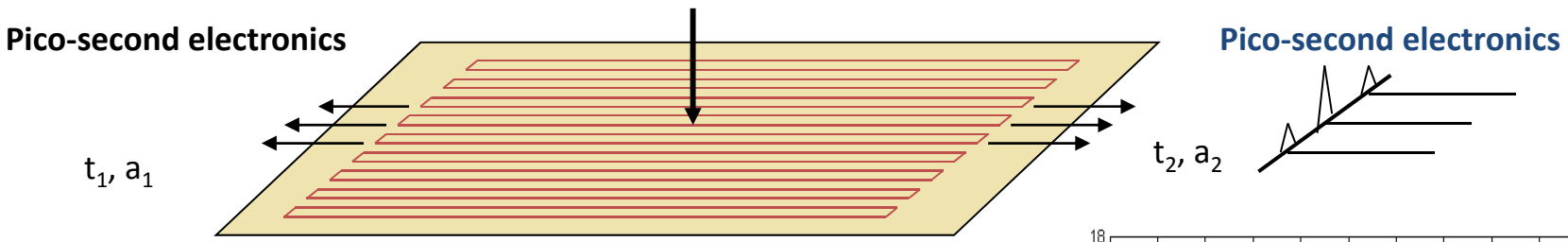
$\sigma_n = \sigma_{n\ det} + \sigma_{n\ elec}$

$$S = G\ Npe$$

Picosecond timing and 2D position for large area detectors: delay lines and Waveform Sampling

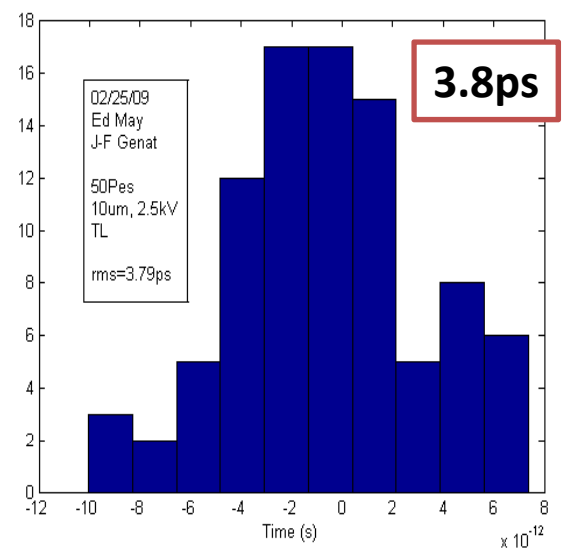
Delay line readout and pulse sampling provide fast timing (2-10ps).
→ Delay lines should have a signal bandwidth matched to the detector

Fewer electronics channels for large area sensors



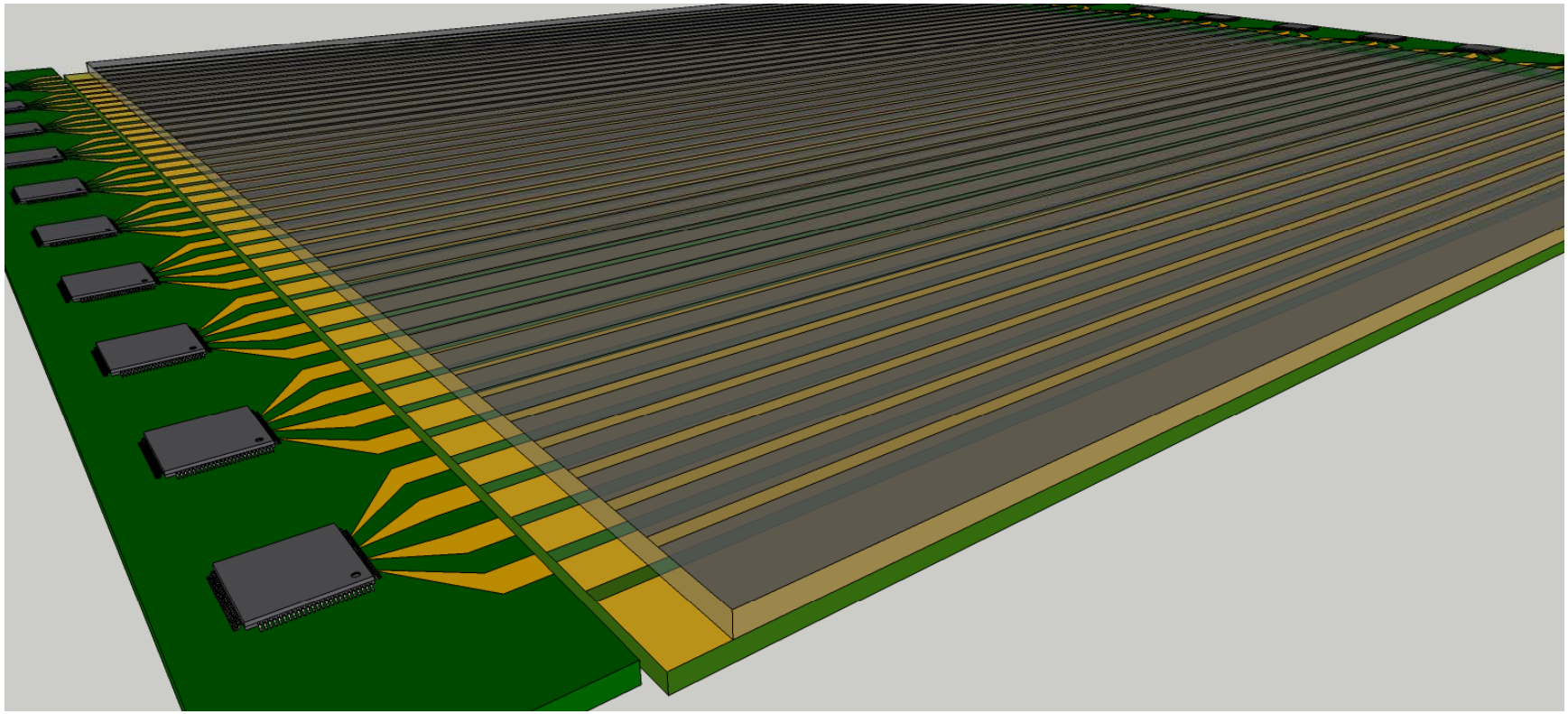
3.8 ps translates in 190 μm position resolution with 50 photo-electrons

½ (t_1+ t_2) = time
v(t_1-t_2) = longitudinal position
$\Sigma \alpha_i a_i / \Sigma \alpha_i$ = transverse position



The electronics contribution to spead is small:
3.8ps / sqrt(2) = 2.7ps,
For 50PEs, MCP is 30ps / sqrt(50) = 4.2ps, equal at 100 PEs

Understanding signal coupling

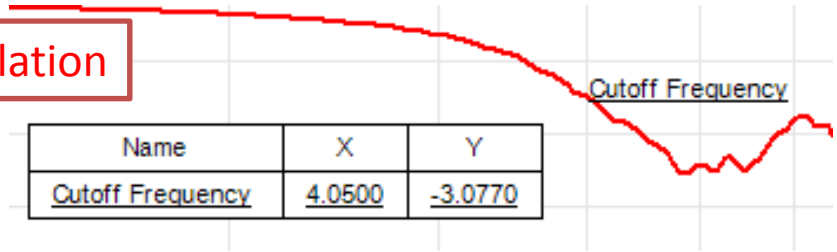


Key issues:

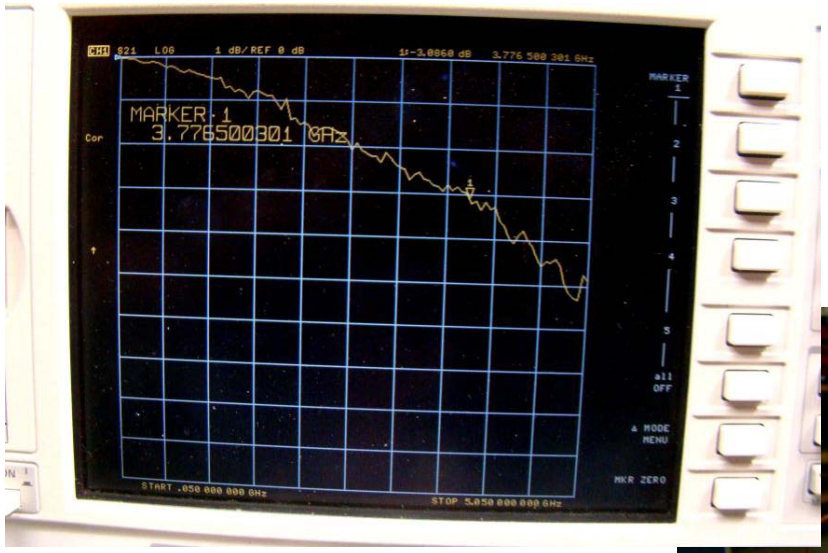
- Optimizing signal coupling (strip width, gaps, impedance)
- Matching analog bandwidth for signal transmission
- Coupling into the readout ASICs

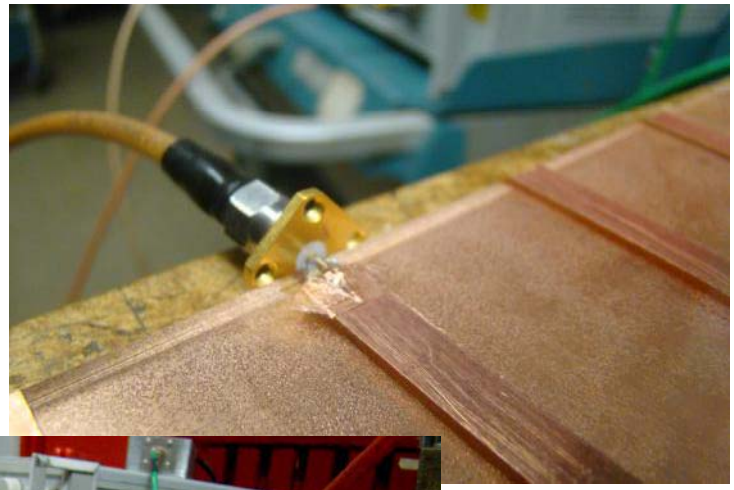
Copper strip testbench

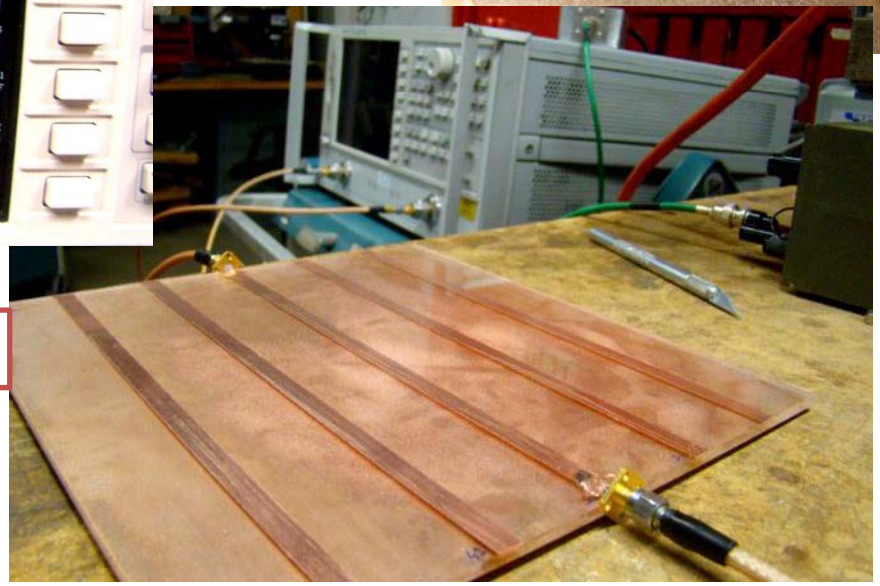
Simulation



Name	X	Y
Cutoff Frequency	4.0500	-3.0770

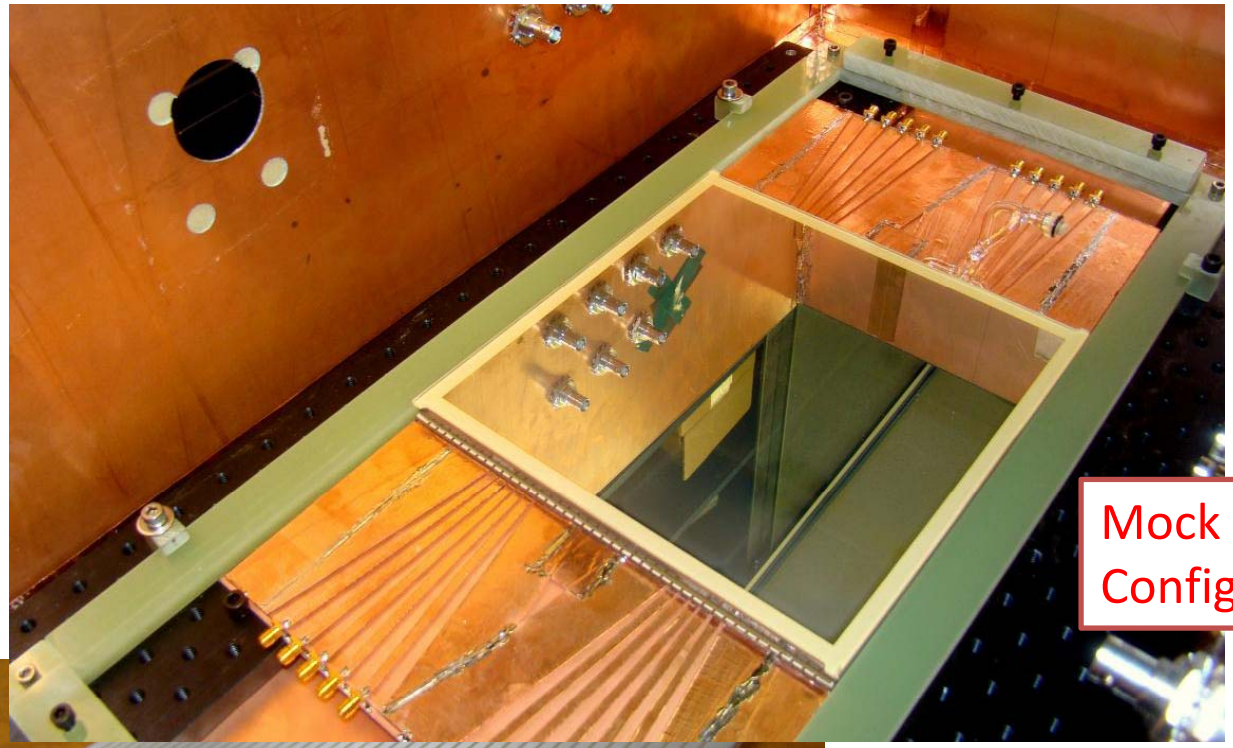




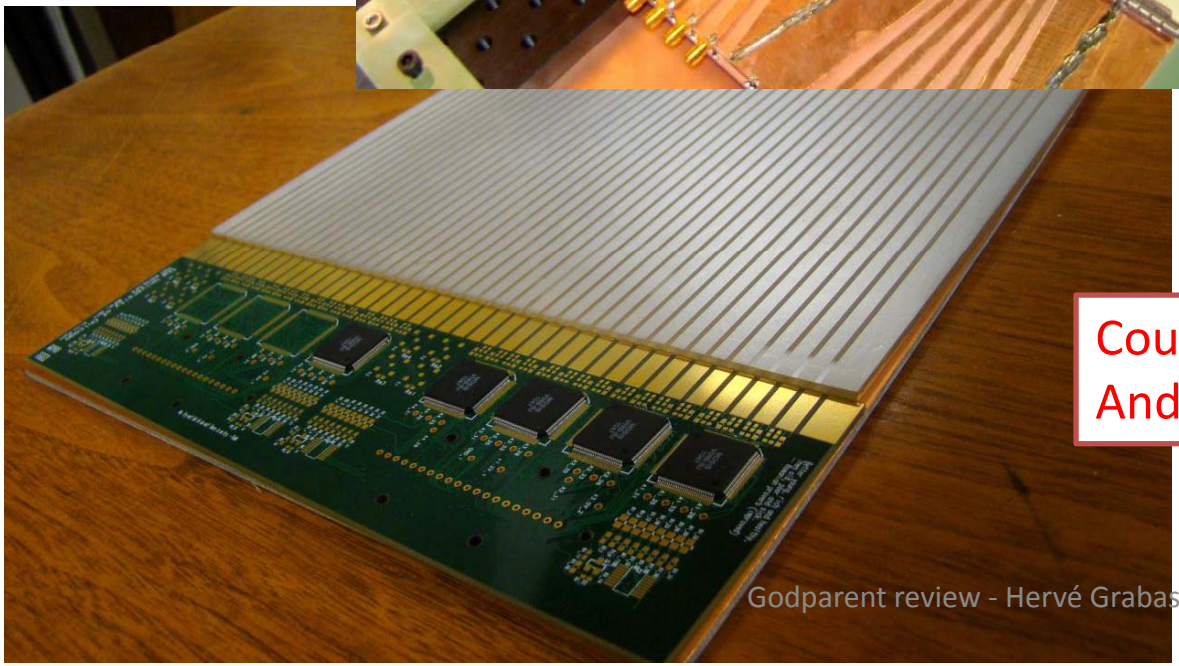


Measurement – good agreement

Important test benches



Mock tile
Configurable strips

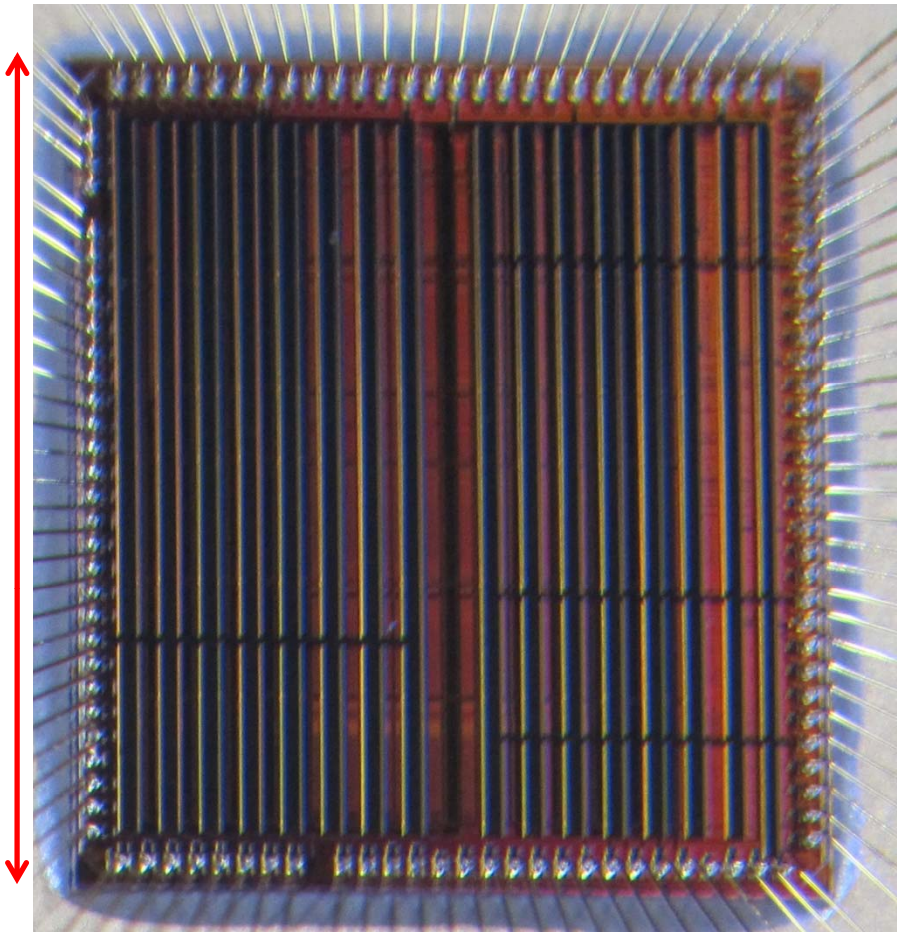


Coupling tests with readout boards
And ASICs, as well as SMA tests

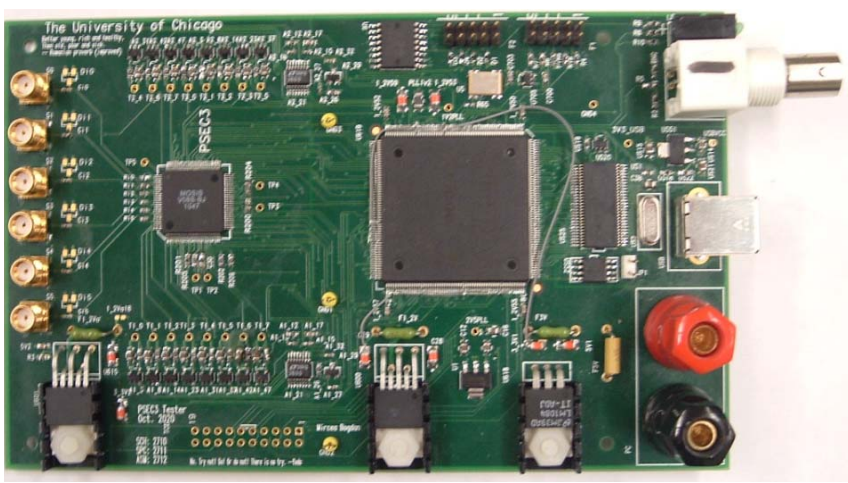
PSEC-3 + PSEC-4 ASICs

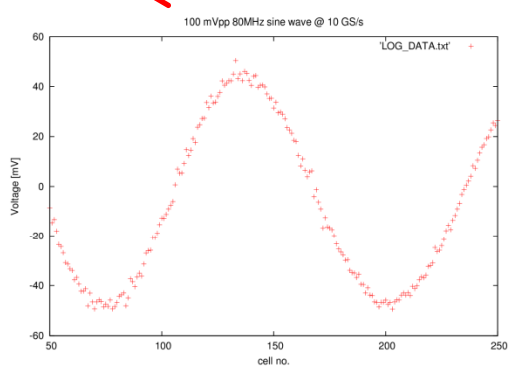
Sampling Rate	2.5 GSa/s-17GS/s
# Channels	6 (or 2)
Sampling Depth	256 (or 768) points
Sampling Window	Depth*(Sampling Rate)$^{-1}$
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz
ADC conversion	Up to 12 bit @ 2GHz
Latency	2 µs (min) – 16 µs (max)
Internal Trigger	yes

4.3mm



4.0mm

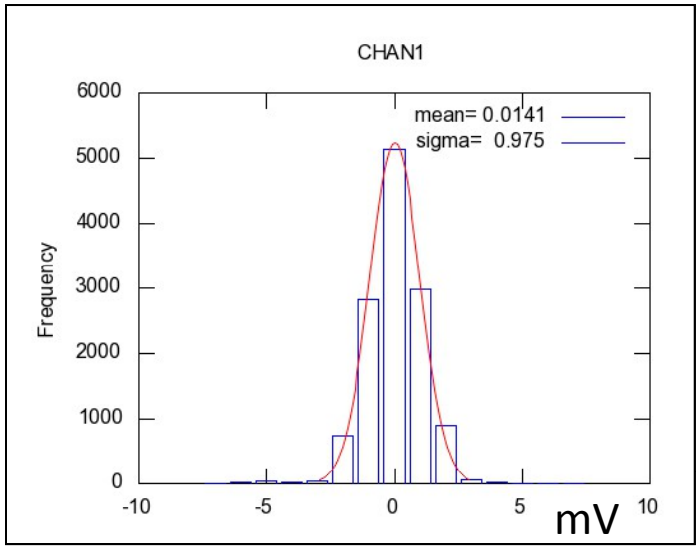




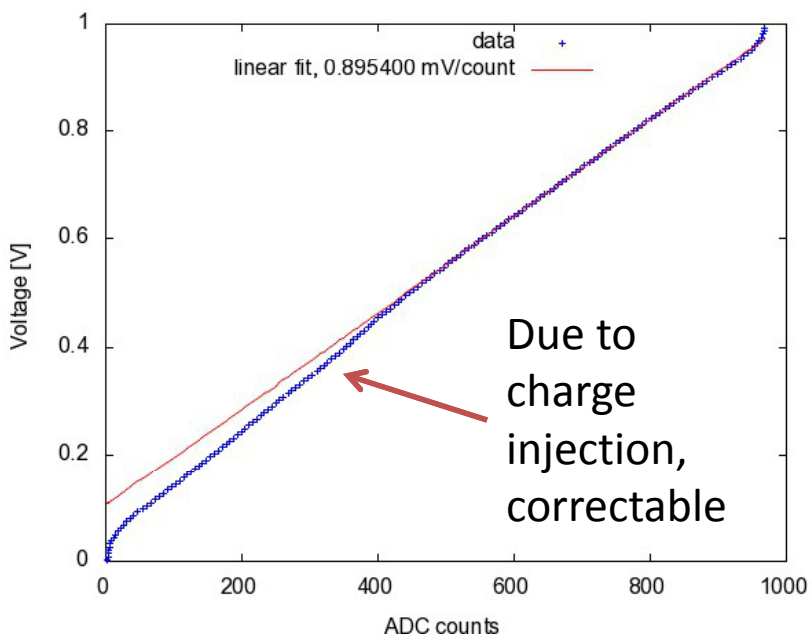
PSEC-3 Noise, linearity, bandwidth

Eric Overla LAPPD Electronics
+ Integration GPC review

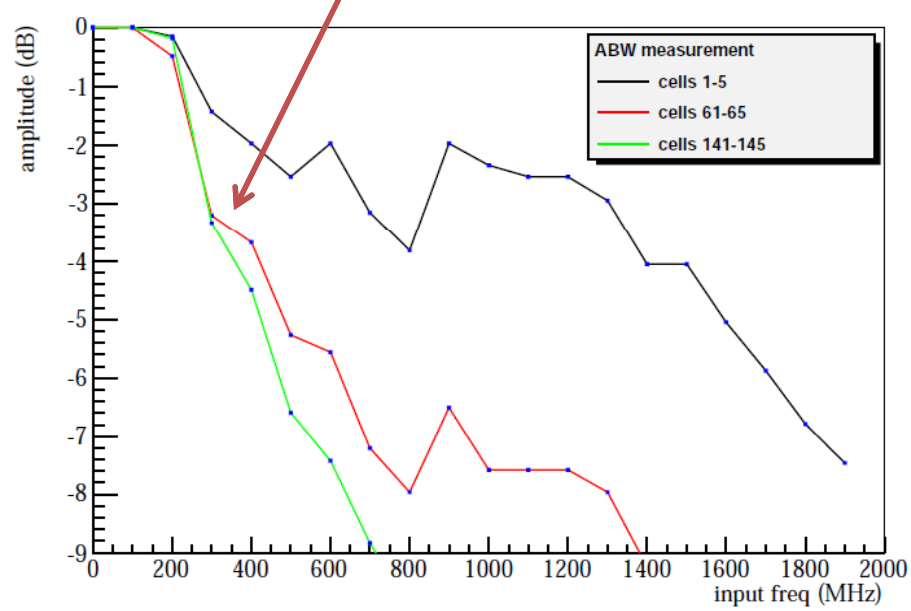
- **Input noise ranges ~1-1.5 mV RMS**
- Dominant source from analog buffers
  - → Issue addressed in PSEC-4 design



PSEC-3 already very usable, PSEC-4 will be even better

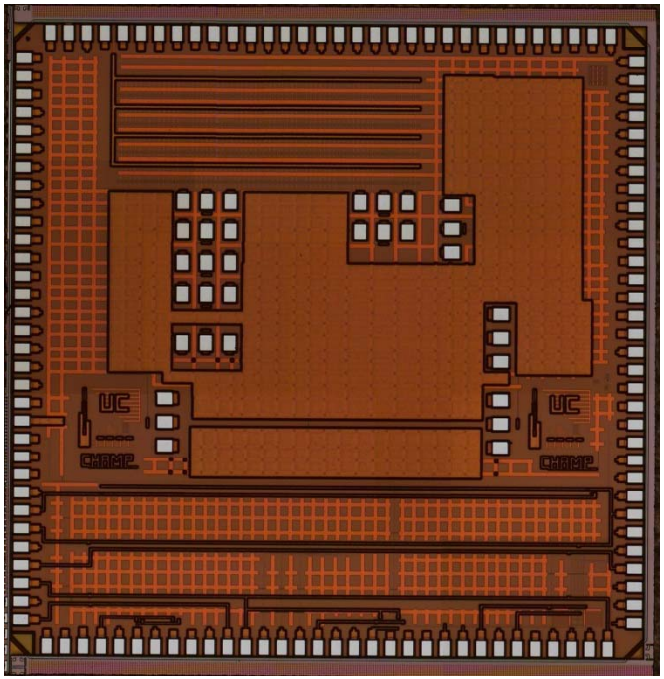


Input bus layout problem – high R, parasitic C

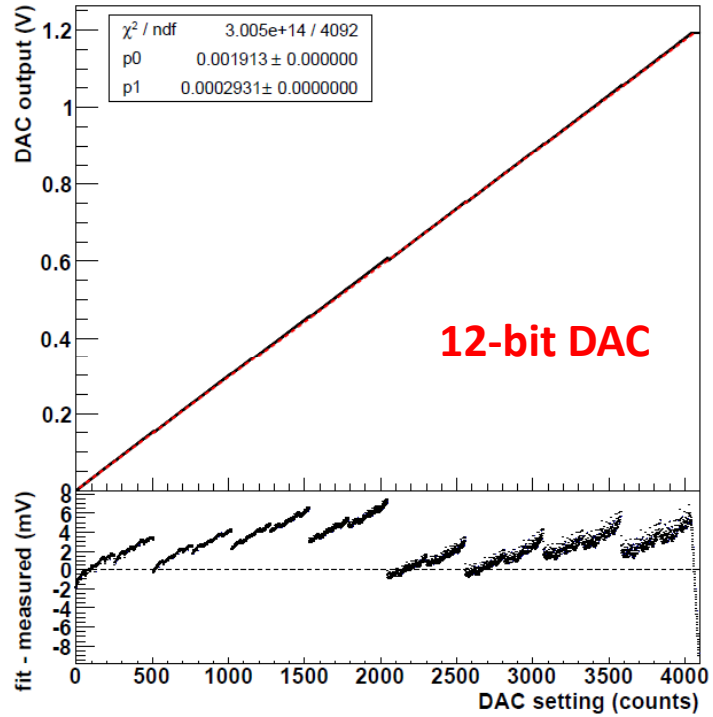


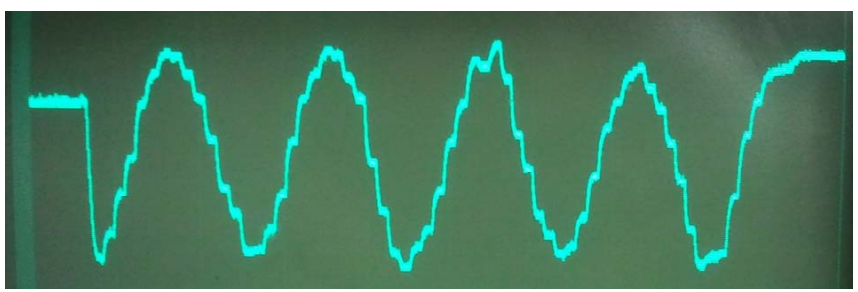
Chicago Hawaii ASIC, Multi-Purpose (CHAMP)

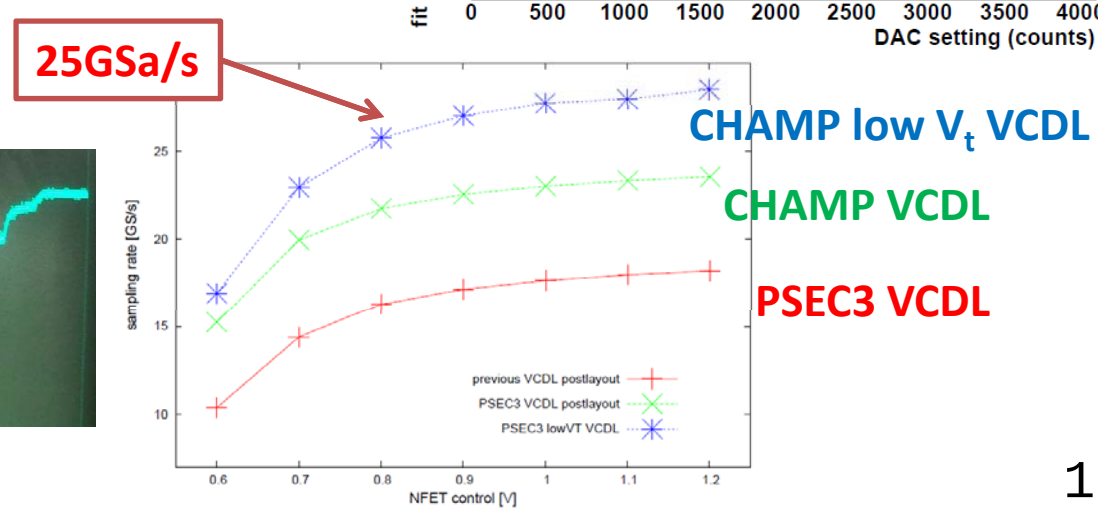
- Develop new circuit elements, train additional students in the IBM 130nm process



Many useful building blocks, will allow increased functionality, more compact implementation







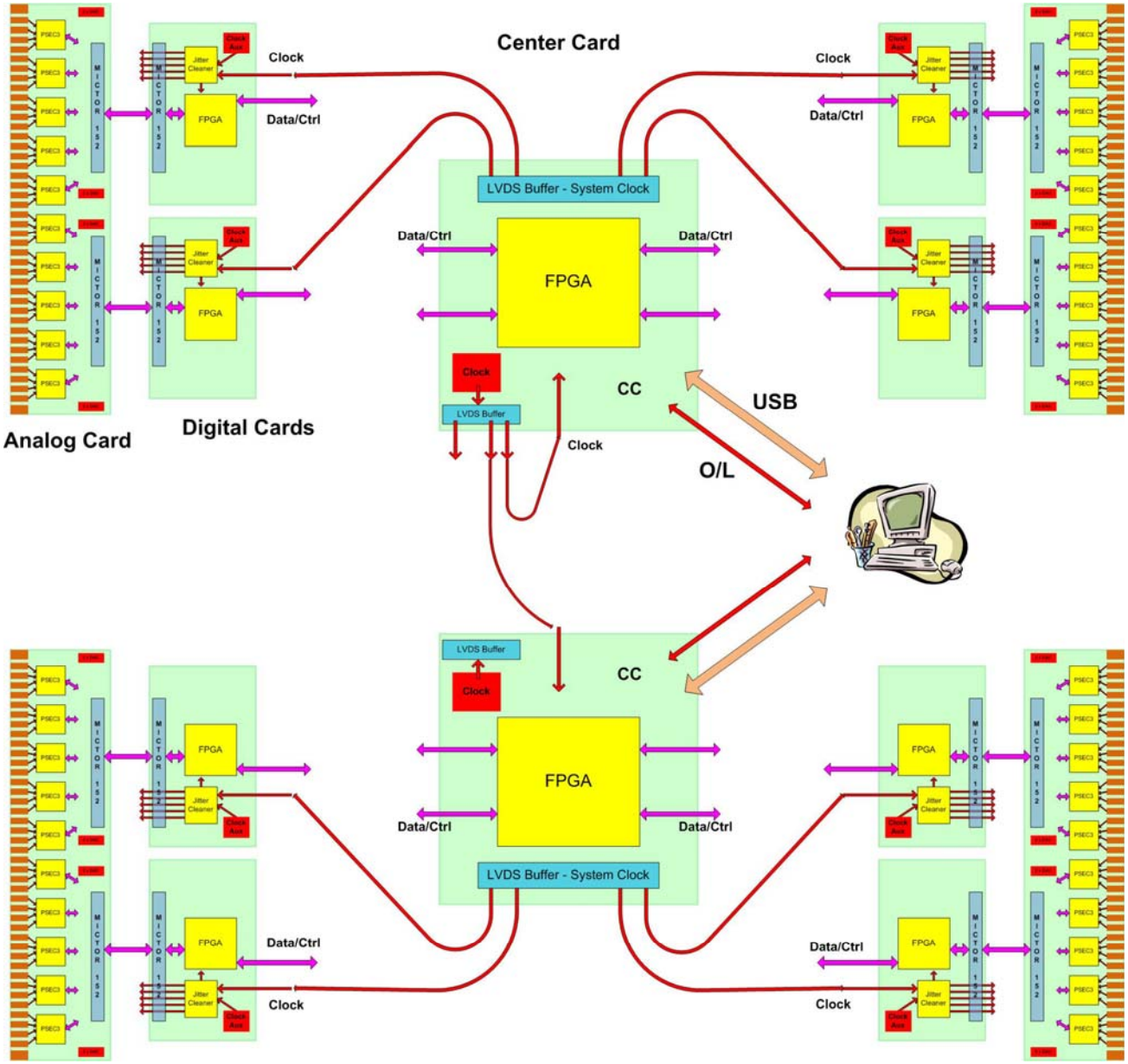
Portfolio of options, leading the way

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

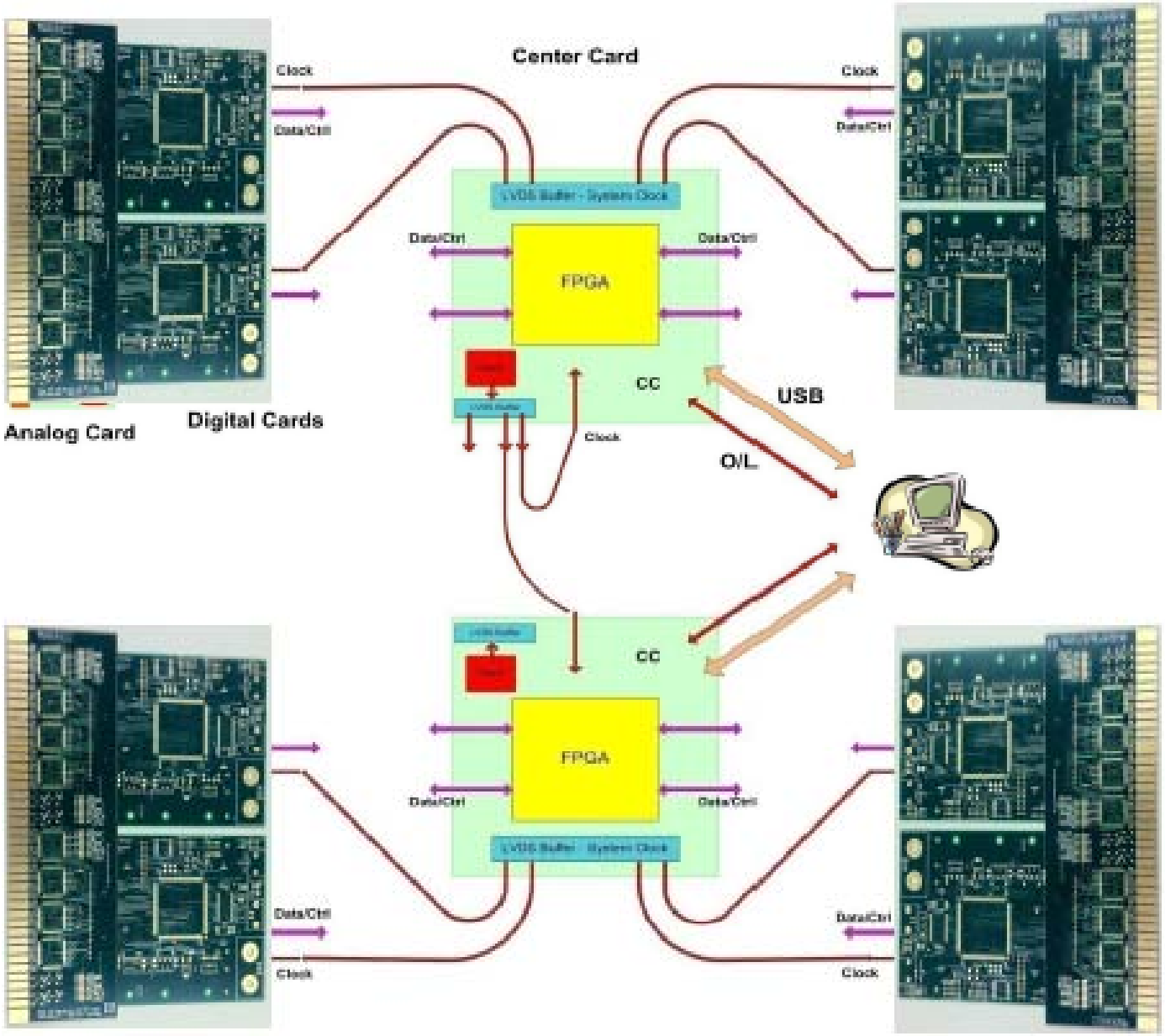
➔ **Success of PSEC3: proof-of-concept of moving toward smaller feature sizes.**

- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

Readout System, beam test configuration



Readout System, beam test configuration

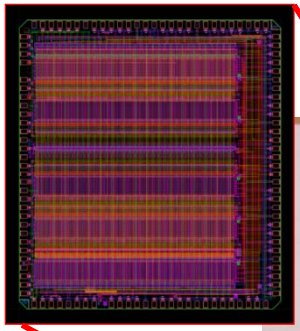


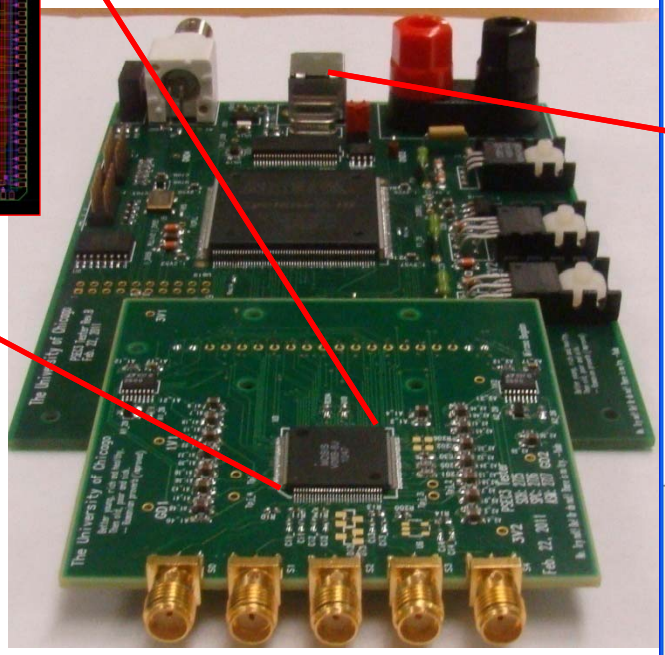
Respin Analog card only for different ASIC

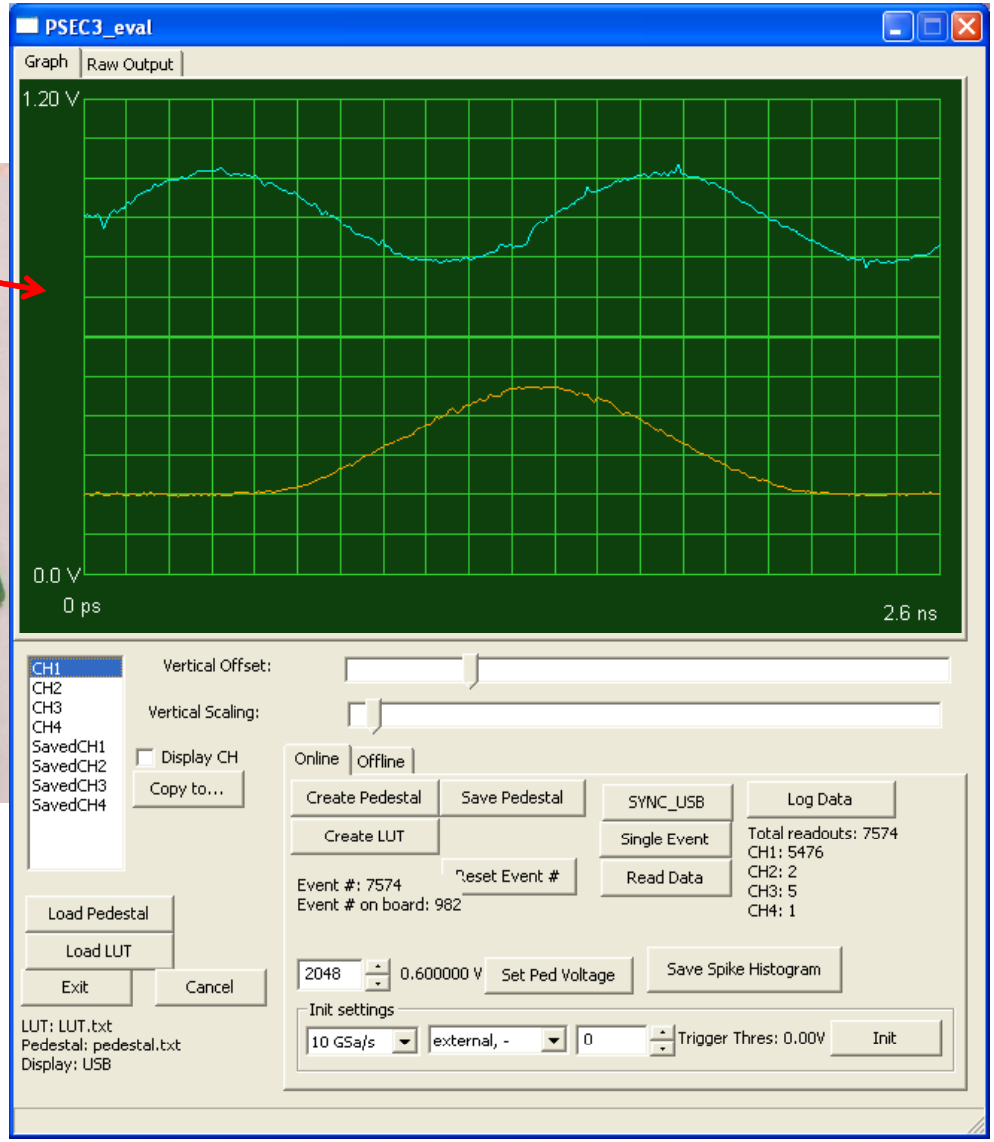
A variety of data collection configurations possible

Demonstrate timing distribution @ ps level between modules

Oscilloscope on a chip? ➔ Calibration







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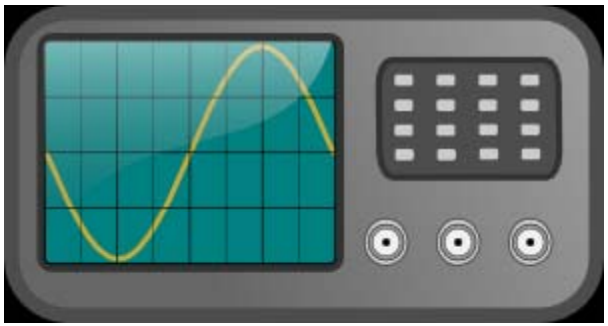
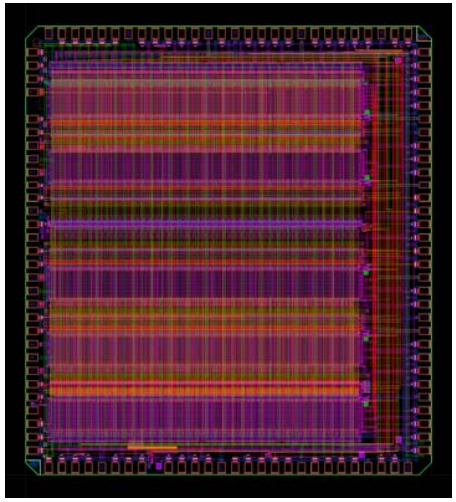


Oscilloscope on a chip? ➔ Calibration

- Modified approximation:



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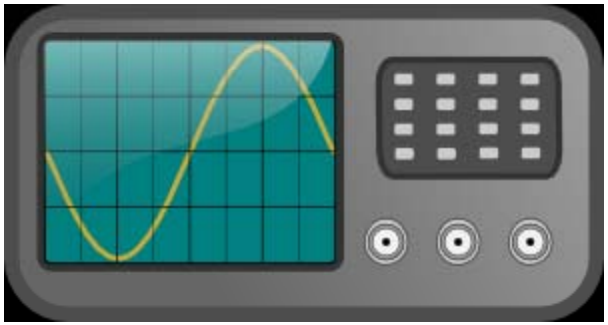
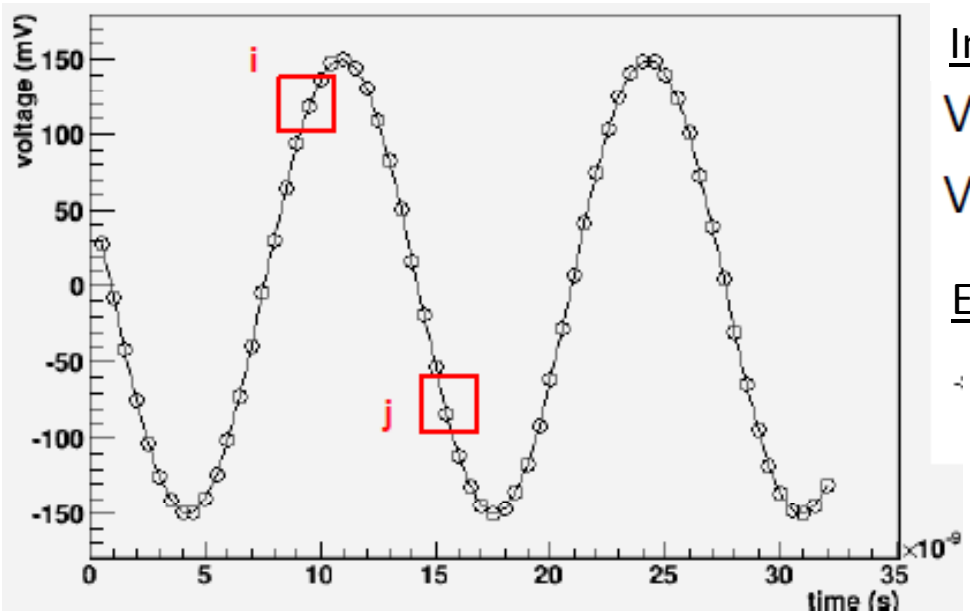


Timing Calibration w/ Correlations

- Plot correlations between pairs of samples:
  - To determine Δt_{ij}, plot $V_i - V_j$ versus $V_i + V_j$



Input signals given by:

$V_i = A \sin(\omega t_i + \phi)$

$V_j = A \sin(\omega t_j + \phi)$

Effectively rotate by 45±:

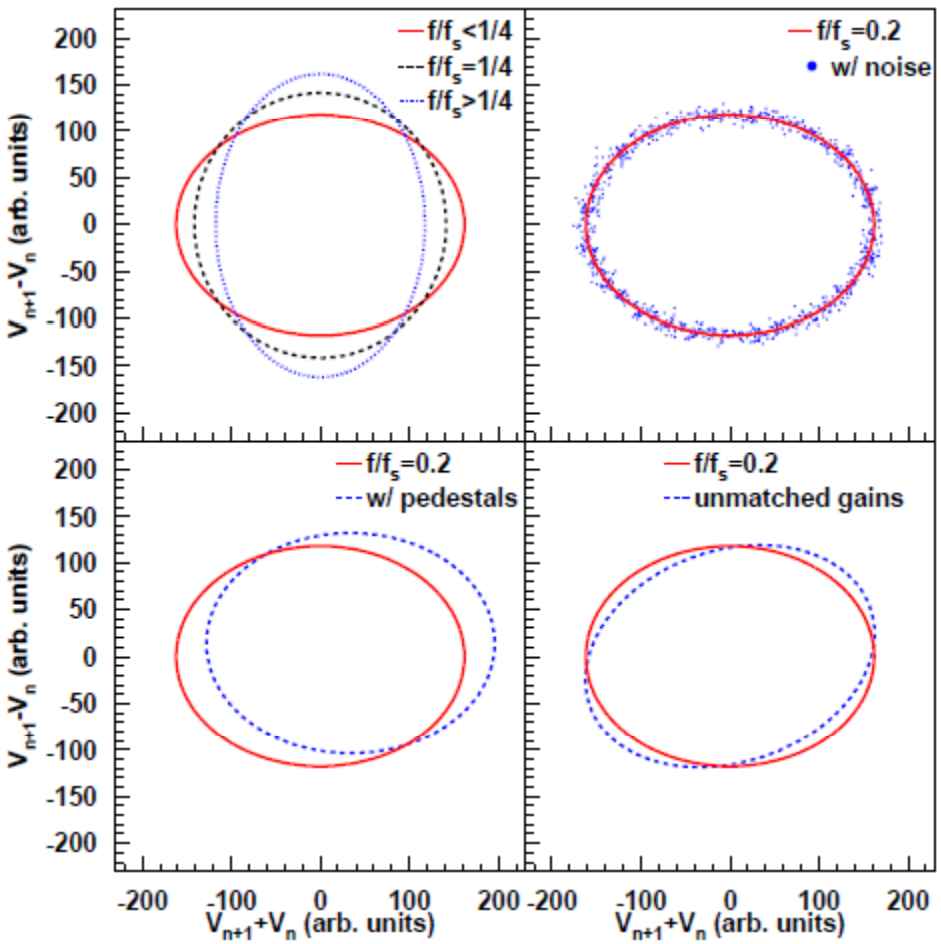
- $x := V_i + V_j$
- $y := V_i - V_j$

➔ $$\frac{x^2}{4A^2\cos^2(\omega\delta t/2)} + \frac{y^2}{4A^2\sin^2(\omega\delta t/2)} = 1$$

- **i and j can be adjacent (or not), but cycle ambiguities exist if > 1 period apart.**

Timing Calibration w/ Correlations

- Ellipse features:

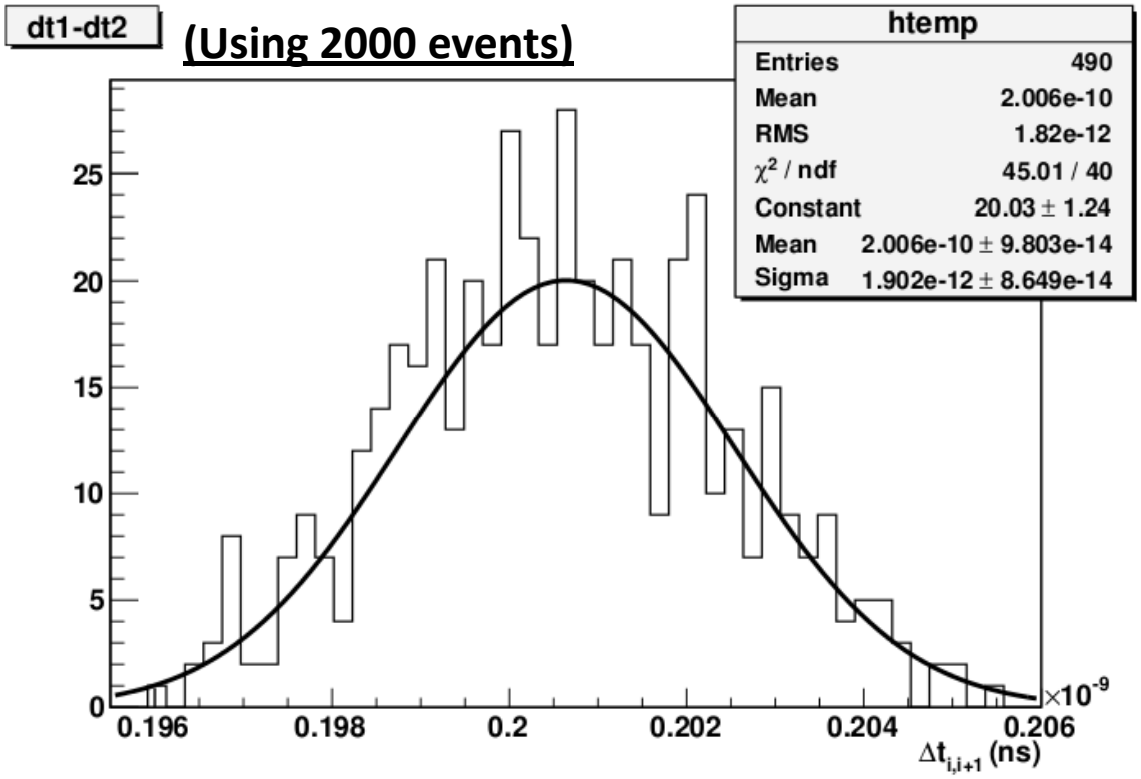


1) Different Δt (for known sampling frequency) give different major/minor radii.
2) Noise makes ellipse "fuzzy"
3) Nonzero pedestals shift origin
4) Difference in gain between two cells causes a rotation.

➔ We have written an ellipse fitter to perform this method.
➔ Even without fitting, it provides nice qualitative check on results.

- **<u>Procedure tested on fast scope data…</u>**

Calculated Δt values for TDS6804B



w/ scope set to 5 GSa/s:

Δt = 200.6 ps

$\sigma_{\Delta t}$ = 1.9 ps

Excellent resolution even with a small dataset.

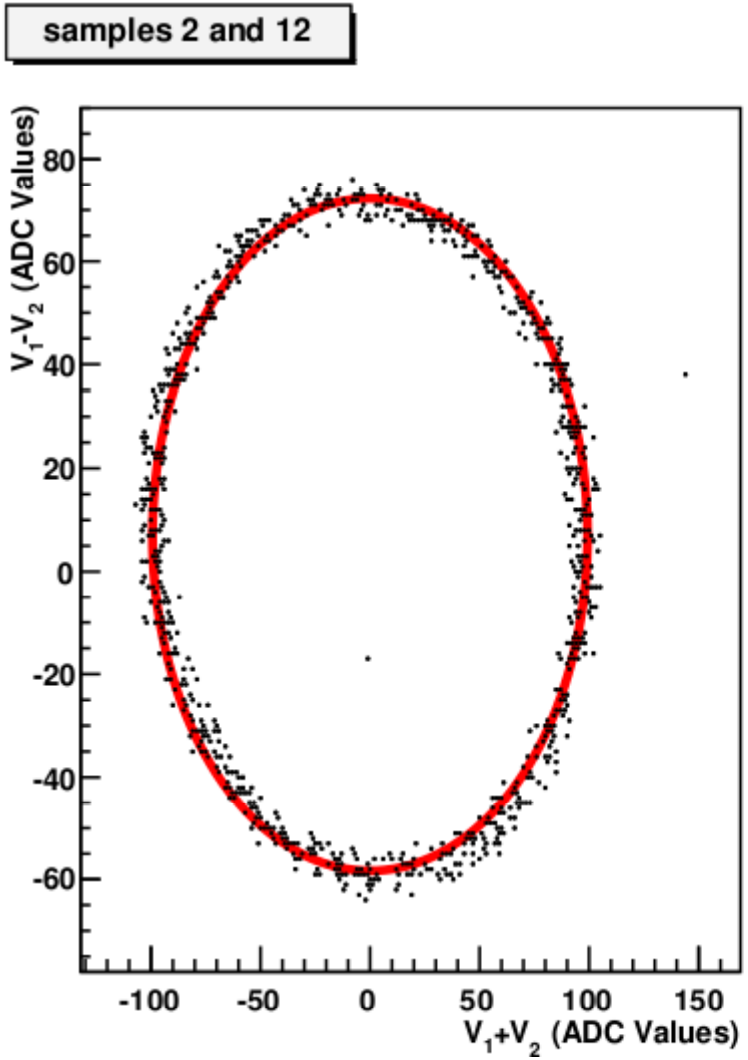
Technique verified… next is PSEC-3 data.

TDS6804B Datasheet

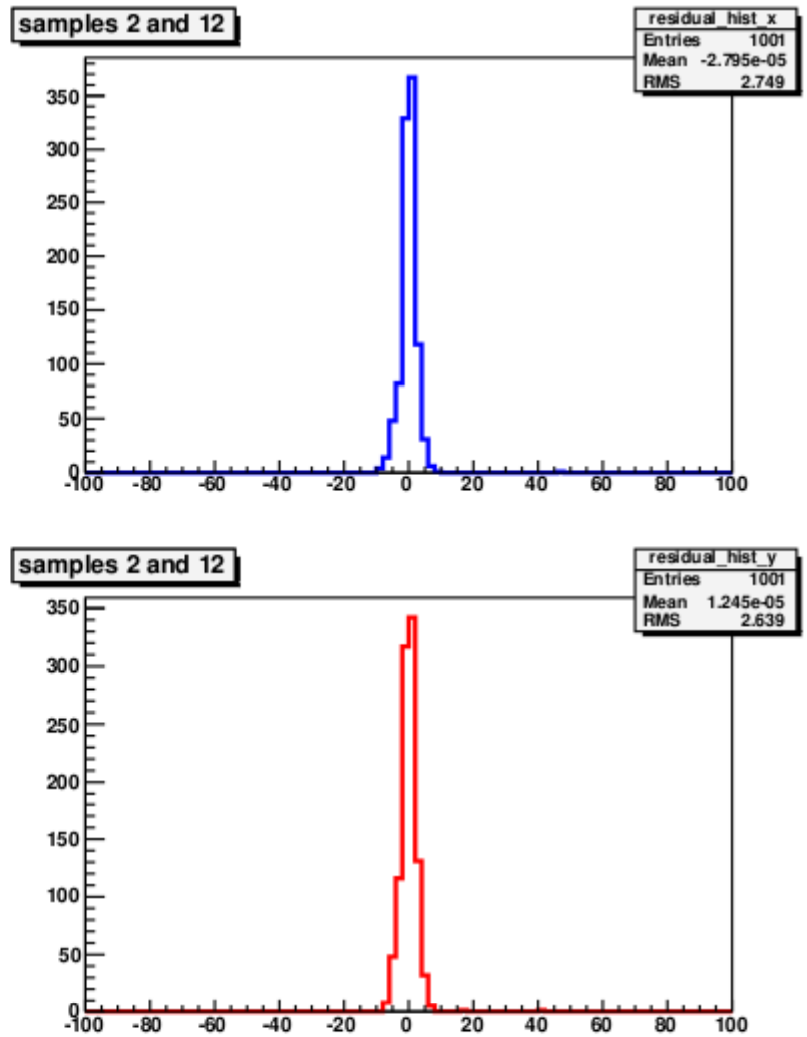
Aperture uncertainty, typical	Short term: ≤1.5 ps rms, records having duration ≤100 ms ≤800 fs rms, records having duration ≤10 μs Long term: ≤15 parts per trillion rms, records having duration ≤1 minute

Example Fit w/ PSEC3 Data

Data and fit

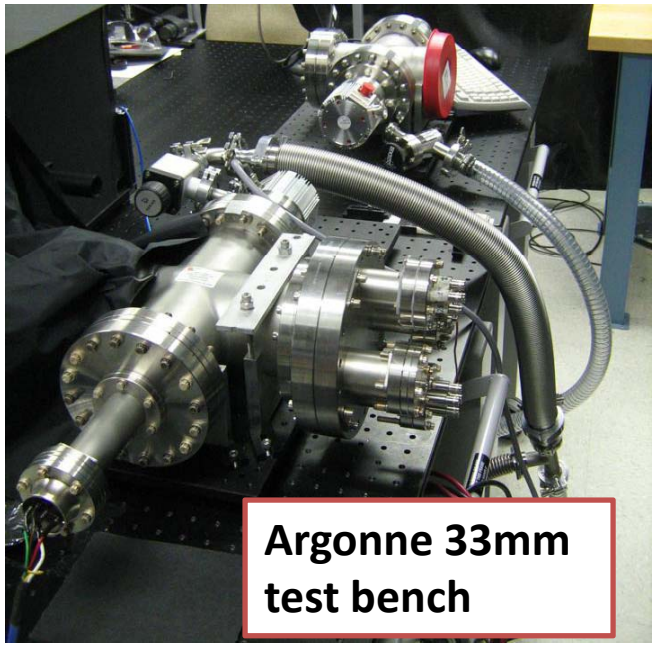


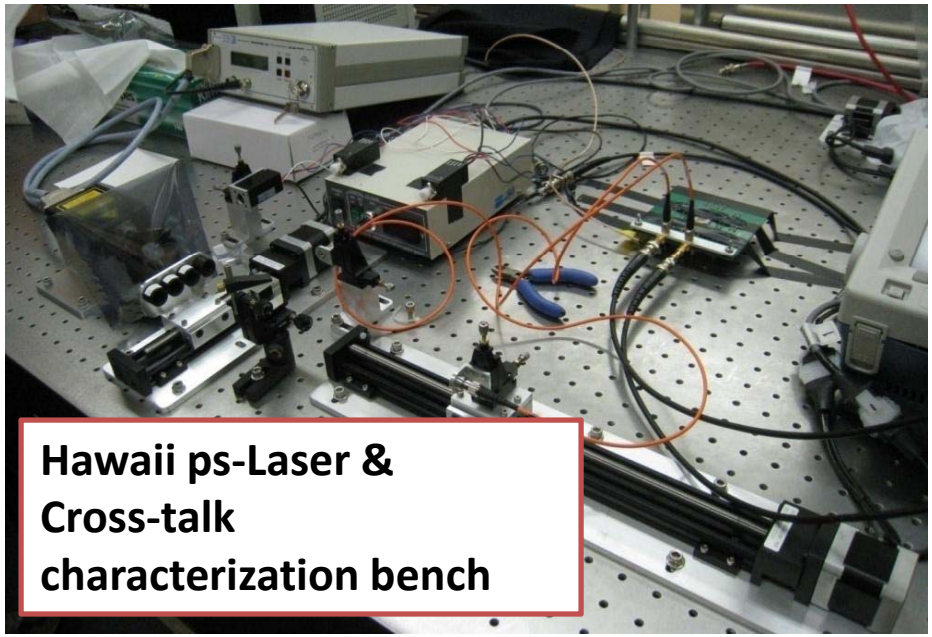
Residuals in x, y

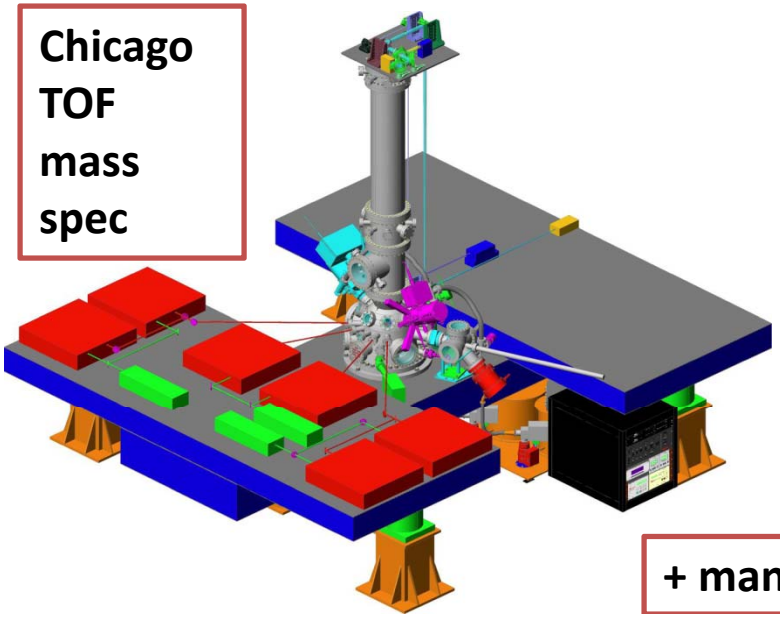


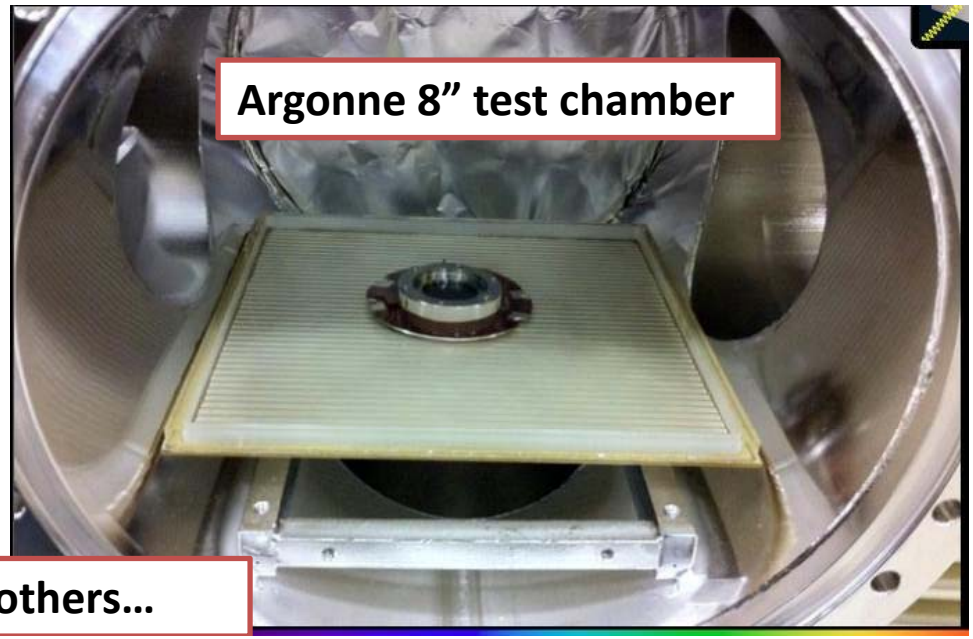
- **Fits are well behaved, converge nicely.**
- **An obvious place to improve: outlier removal.**

Next steps – outfit various test benches









+ many others…

Some highlights – since last godparent review (6 months)

1. Further understanding of the processes that limit timing resolution http://psec.uchicago.edu/workshops/fast_timing_conf_2011
2. A much more fundamental understanding of how to couple the charge signal into the readout anodes
3. Understanding how to make a electrically and mechanically viable readout
4. First and impressive test results with the PSEC3 and submission of PSEC4, to clean up a few, minor bugs
5. Expanded significantly expertise with the IBM 130nm process and tested future subcircuits on the CHAMP ASIC
6. Fabrication of ASIC evaluation boards, as well as the first tile/module scale readout boards
7. Exploration of options for large-scale/high-speed readout, with a number of viable solutions identified
8. Evaluation of calibration procedures, required constants, and data archiving

Electronics Summary

- Steady progress, resource bounded
- Currently no show-stoppers
- Will learn much from first integrated readout tests
- Field-test experience of readout systems at ANL, Chicago and Hawai'i
- Building toward full system (timing) beam-test