SOI pixel research and semiconductor Lab at IHEP

Yunpeng Lu

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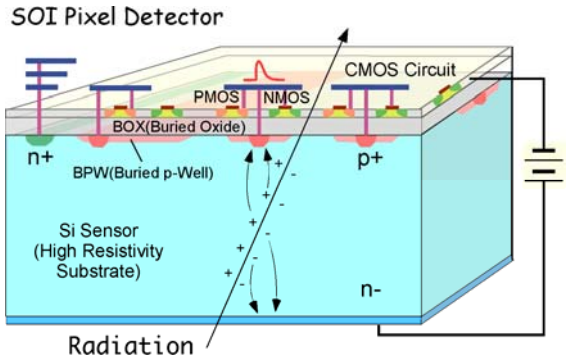
A thread going through this talk

- How this business got started &
- How it is going

Background

- A beginner in silicon pixel
  - Worked on PCB, FPGA, OPAMP as a graduate student and post doctor.
  - Spent almost one year working with FE-I4 team at LBNL—getting closer to silicon pixel.
  - Started design and test of a SOI chip one year ago–hands on it finally.
- IHEP has been supporting silicon pixel in recent years.
  - Enhance manpower
  - Upgrade facility

SOI pixel for X-ray imaging

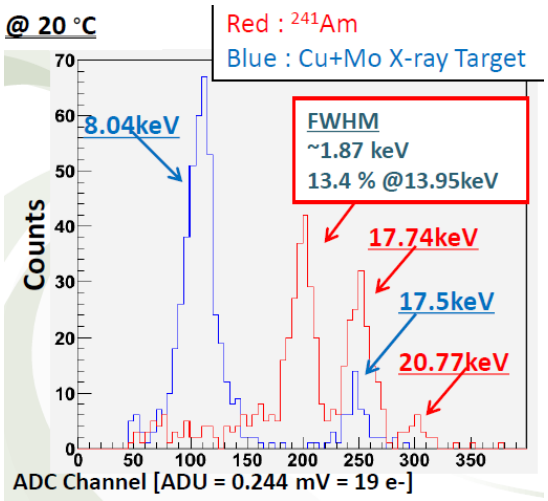


- Advantages:
  - Monolithic, no bump bonding.
  - Full depletion, direct detection of X-ray.
- Problems to be solved:
  - Radiation hardness, can't meet the requirements for a collider, but OK for synchrotron light source, dental imaging and mammography.
  - Cross talk between circuit and sensor, digital circuit injected charge to sensor by capacitive coupling, but integrating circuit works well by far.
- SOI pixel is most likely to be applied in X-ray imaging.

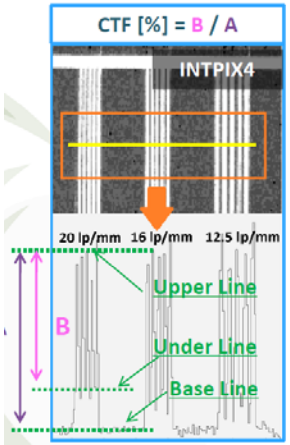
SOI MPW run in Japan

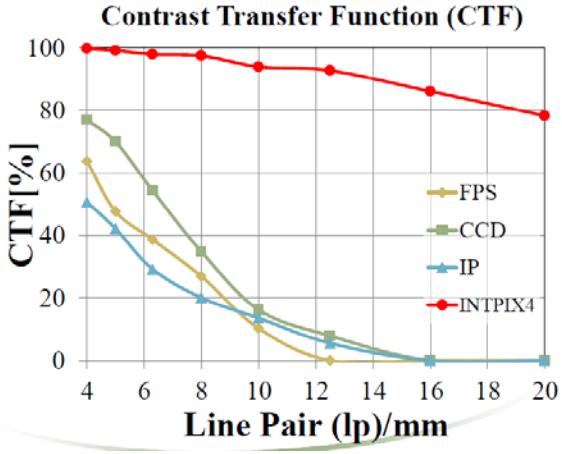
- Pro. Yasuo Arai at KEK organizing a world-wide collaboration and offering MPW run with IC company LAPIS.
- This unique institute-corporation joint force works quite well.

X-ray Energy Spectrum

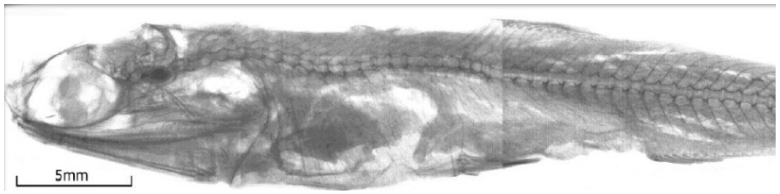


Mo: molybdenum





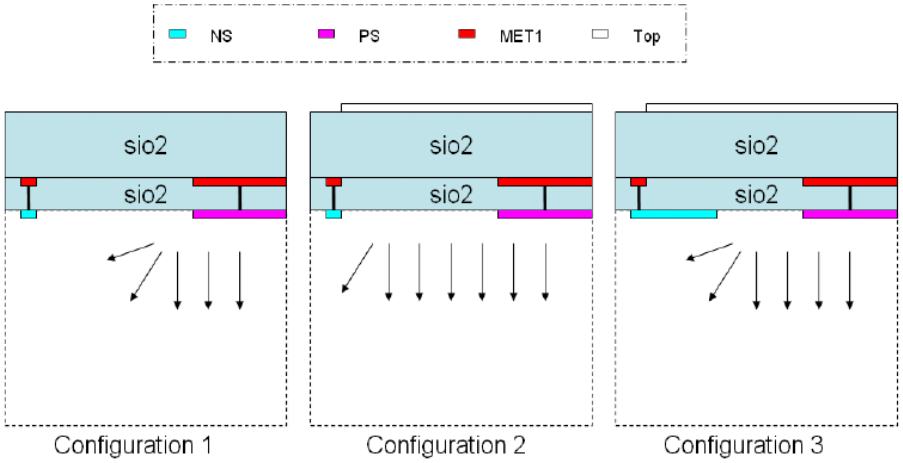
X-ray Imaging of a Sardine



Note: These figures are from Ayake Taketa at KEK.

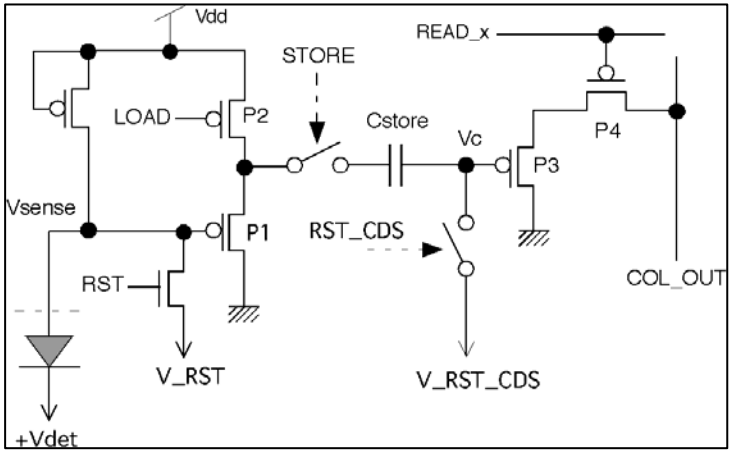
My first try on SOI pixel

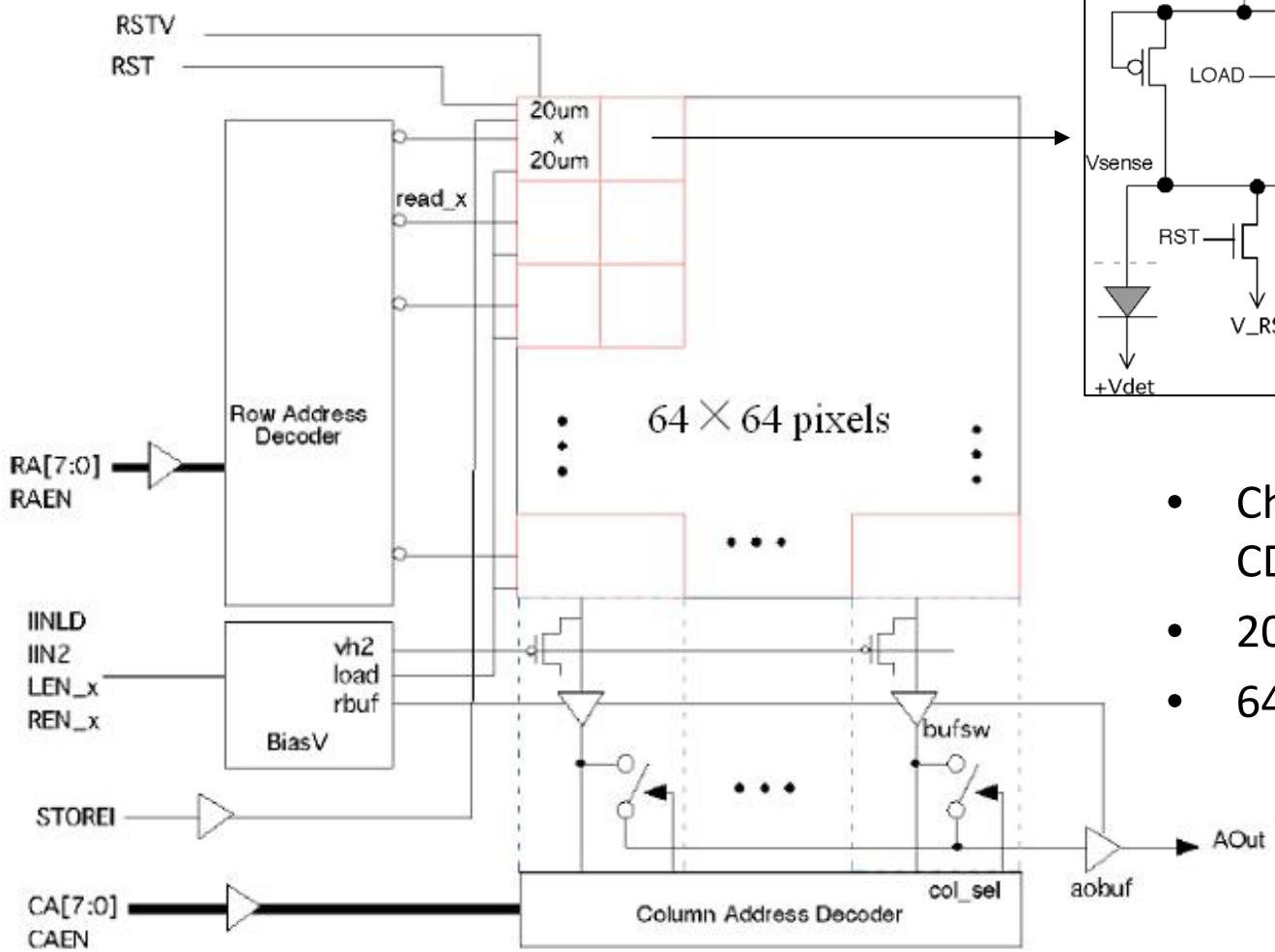
- I asked to join and received a warm welcome.
- I went to KEK for a 3 month visit and completed a small but equipped-with-full-function chip. Aimed at
  - Higher dynamic range by replacing Core transistor with IO transistor, voltage swing increased from 1.2V to 1.8V.
  - Faster readout by tuning the circuit carefully, 100ns/pixel.
  - Improving the HV breakdown by introducing new edge structure.



Circuit block of the chip

Pixel Circuit

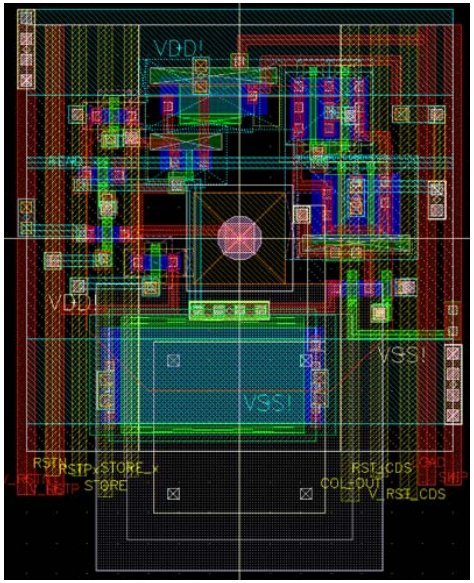




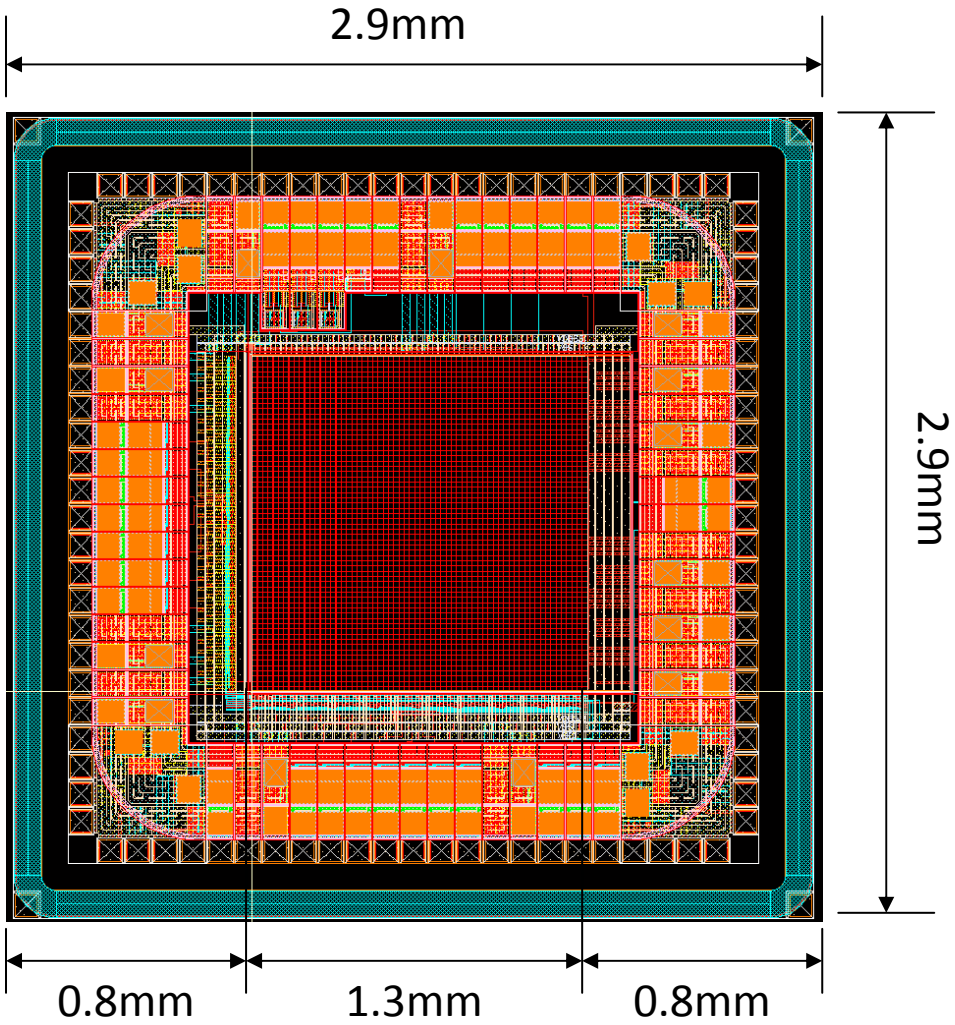
- Charge integrating, CDS
- 20um*20um pixel
- 64*64 array

Layout

- 2.9mm*2.9mm
- 72 Pads surrounding
- 20% of total area sensitive



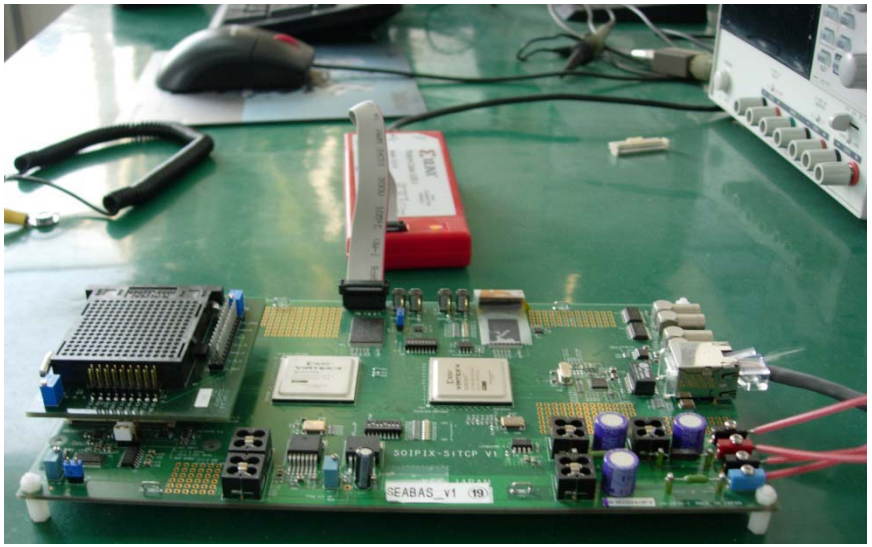
Single Pixel layout



The chip layout

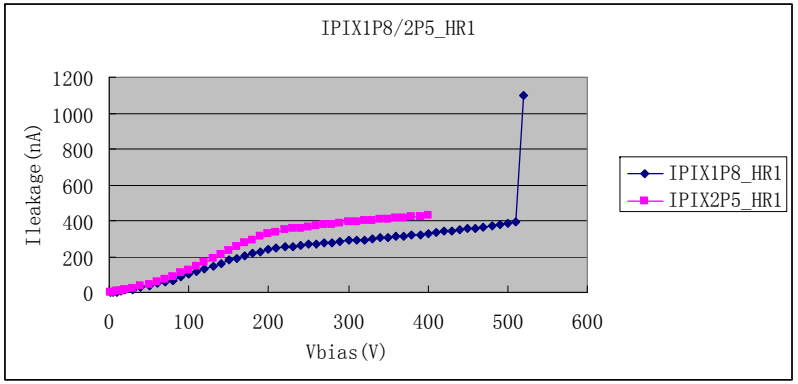
Test Setup

- Keithley source meter: HV bias and I-V test.
- Major component: SEABAS (Soi EvAluation BoArd with Sitcp) from KEK. Encrypted TCP/IP firmware.
- Sub-board, FPGA coding.
- Software (Nice work by Yi Liu).



Play with the chip

- Got the chip back in March.
- Power up
  - Voltage on with reasonable current, a good start.
- Check the response of digital circuit
  - Responds as expected, a piece of silicon communicating with outside world!
- Full control of the chip
  - Seems in good order.
- Bias the sensor, make a I-V curve
  - HV up to 500V can be applied, while 300V should deplete the 260um substrate completely.

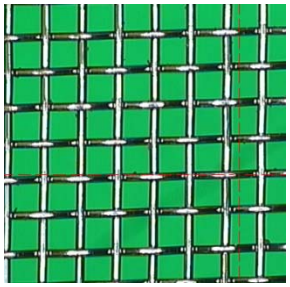


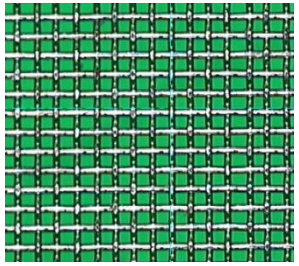
- Took images with red pointer as source
  - 4um*4um window for light illumination in each pixel.

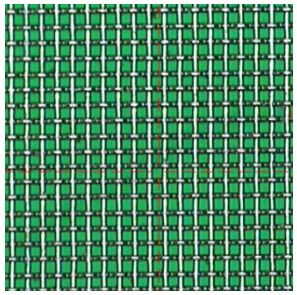
Red Light Imaging of Metallic Mesh

159um pitch | 79um pitch | 64um pitch

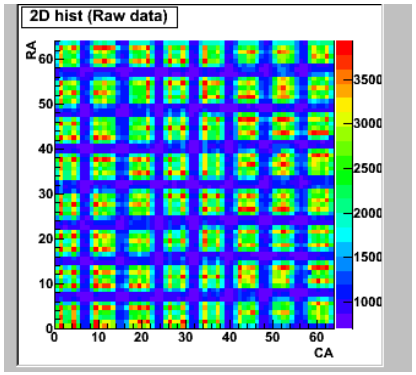
Microscope pictures

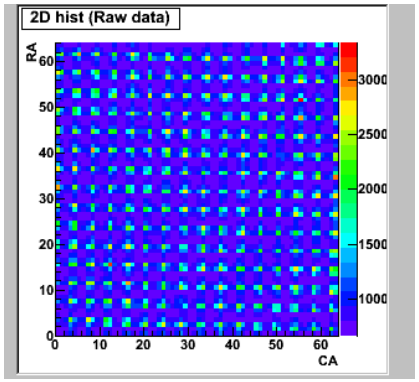


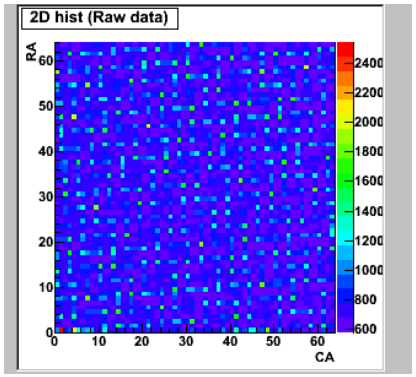




Images taken by the chip

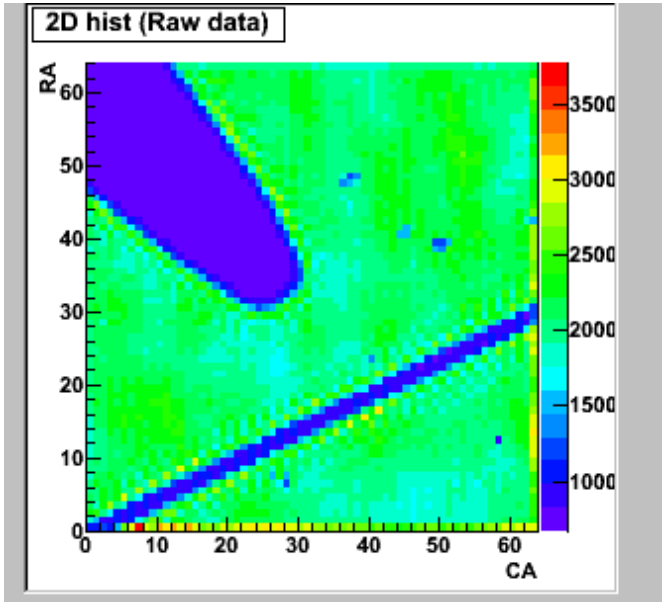






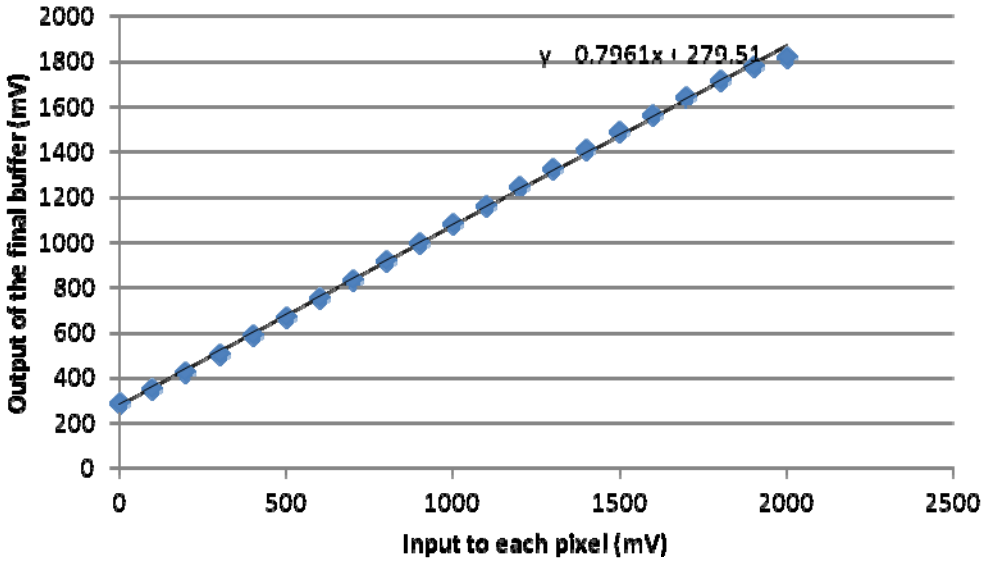
Red Light Imaging of small objects

- The tip of a pin and 30um golden wire.
- The saw-teeth is a proof of good response to light.
  - 20um*20um pixel.



Characterize the chip quantitatively

- Calibrate the circuit
  - Gain=0.7961
  - Dynamic range > 1.8V



Measure the Capacitance in pixel

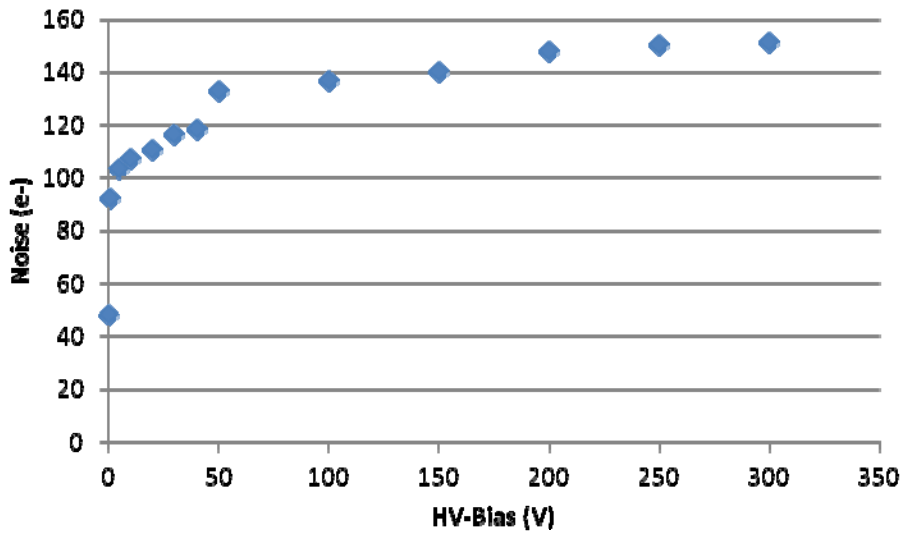
- Integrating leakage current for a period of 250us results in 340mV.
- Leakage current 70nA in total for 4096 pixels.

$$Cd = \frac{\Delta Q}{\Delta V} = \frac{\frac{70nA}{4096\ pixels} \times 250us}{340mV} = 12.6fF$$

- Conversion Coefficient = 1/Cd = 12mV/1000e-

Noise as a function of HV Bias

- Measure the integration of leakage current for 100 times, take the standard deviation as noise.
- Noise increases with HV bias, around 150e- when fully depleted.



Outlook on this work

- Leakage current needs to be understood.
- X-ray imaging test is in planning.
- SOI detector should be able to achieve:
  - Up to 700um thickness full depleted
  - Frame rates: 1K frame/s
  - Full well depth: 150K e- @ 20um□pixel
  - Noise: 100e-

Semiconductor Lab to build at IHEP

- Cleanroom
  - 140m^2
  - Class-10,000
  - Temperature control: **±1°C**
  - Humidity control: **±10%RH**
- EDA software
  - Already have license for PCB and IC
  - License for TCAD will be ready soon.
- Instruments and equipment
  - Probe station
  - Wire bonder
  - Bonding tester
  - semiconductor inspection microscope
  - Robotic dispenser
  - Coordinate Measuring Machine

Budget has been approved.

Thanks for your attention.