PSEC4 ASIC Update
(much deferred to Mircea's talk)

Eric Oberla, Joachim Cohen

(many, many others…)

on behalf of the LAPPD Electronics group

LAPPD Electronic GP Review – 9-JUL-2012

HIGH ENERGY PHYSICS

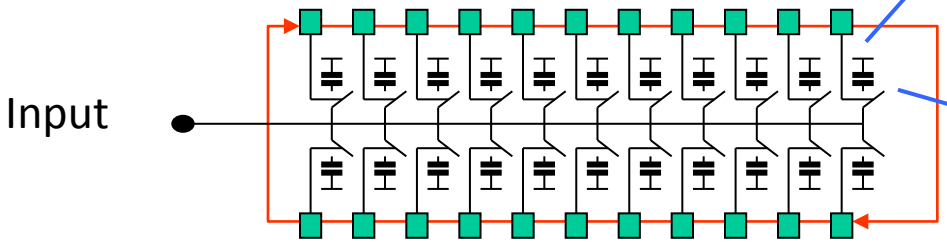
THE UNIVERSITY OF CHICAGO

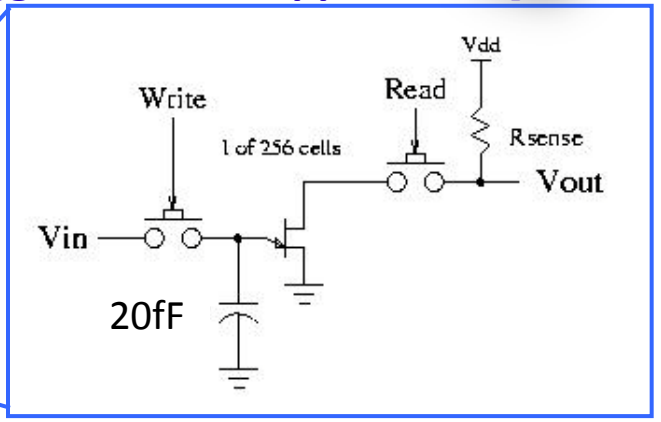
Switched capacitor array sampling: '*analog down-conversion*'

LAPPD Collaboration

[GHz sampling→ 10-100 MHz readout: useful in most 'triggered event' applications]

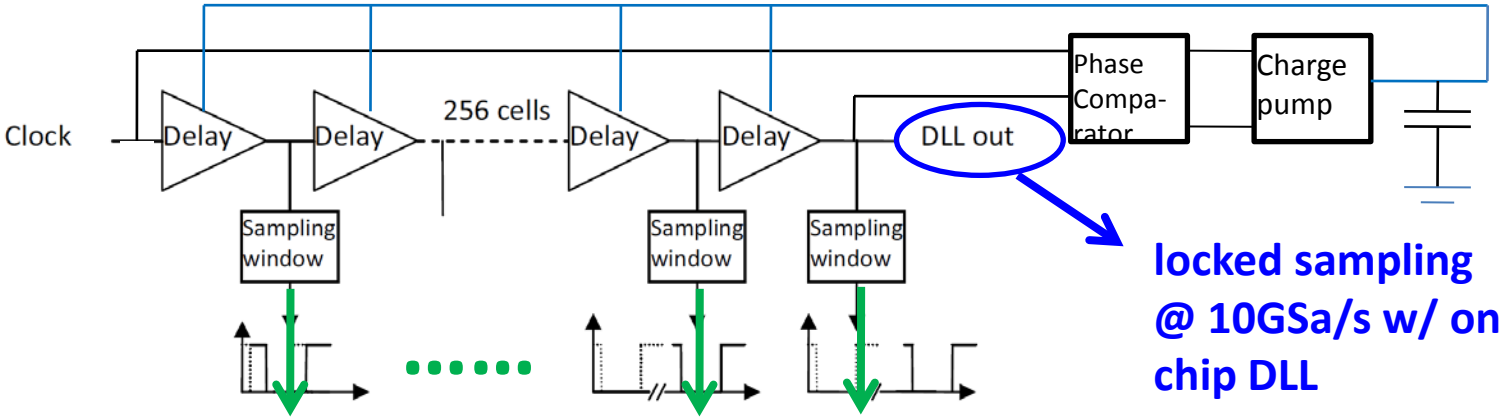
Write pointer passed along array - generates 'sampling window' (~5-10 switches closed at once):





Tiny charge: 1mV ~ 100e$^-$

Timing generation with a delay locked loop (DLL):



locked sampling @ 10GSa/s w/ on chip DLL

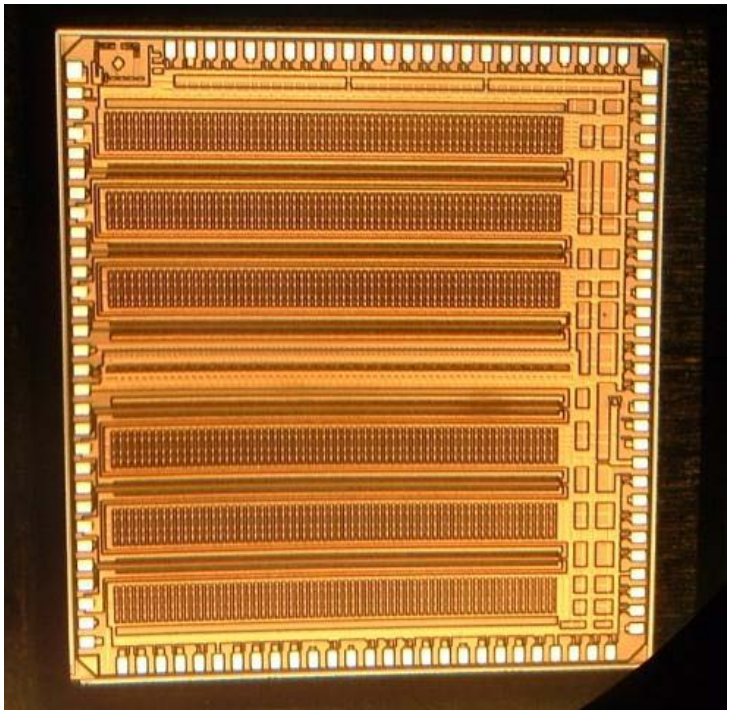
To switched capacitor array – sample & hold

PSEC-4 ASIC

LAPPD Collaboration

10-15 GSa/s Waveform Sampling ASIC

	ACTUAL PERFORMANCE
Sampling Rate	2.5-15 GSa/s
# Channels	6
Sampling Depth	256 points (17-100 ns) per channel
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz (f_{3dB})
ADC conversion (ramp-compare)	Up to 12 bit (10 ENOB) clocked @ 1.6 GHz
Dynamic Range	0.1-1.1 V
Readout Latency	2 µs (min) – 16 µs (max)

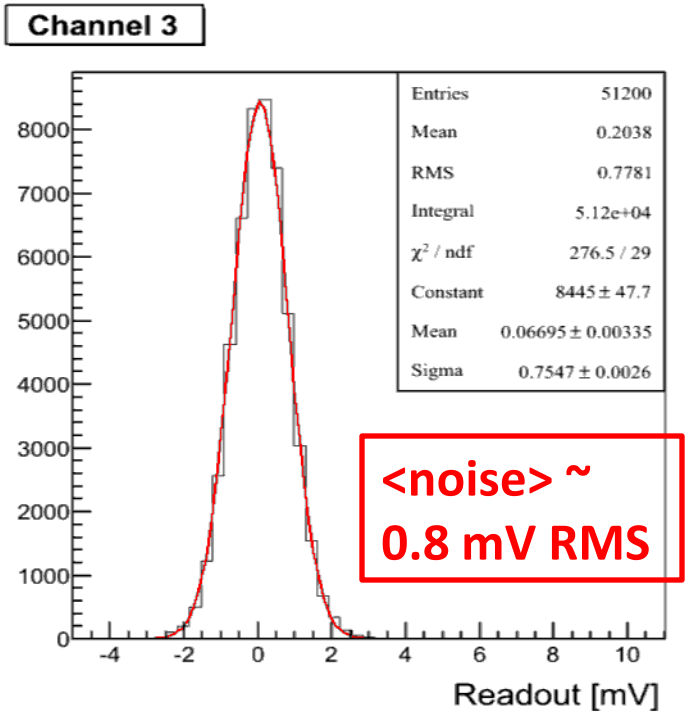


Designed to sample & digitize fast pulses (MCPs):

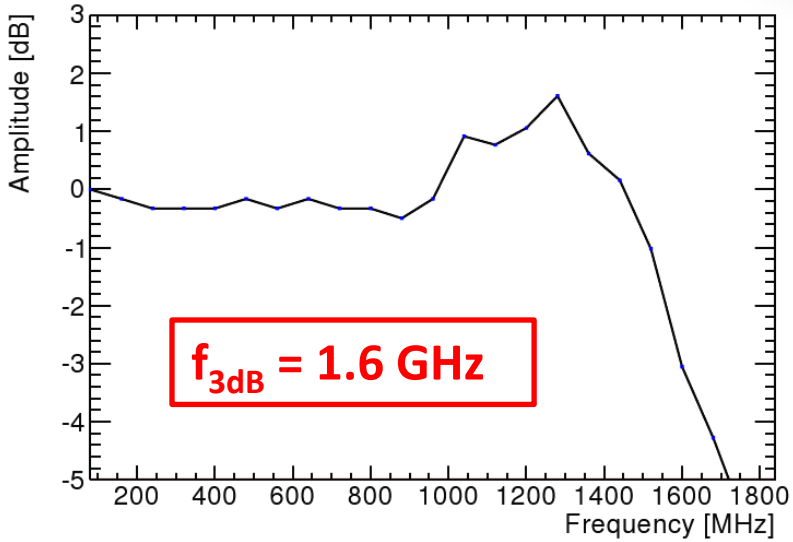
- Sampling rate capability > 10GSa/s
- Analog bandwidth > 1 GHz (challenge!)
- Relatively short buffer size
- event-rate capability ~100 KHz

→ ***130 nm CMOS***

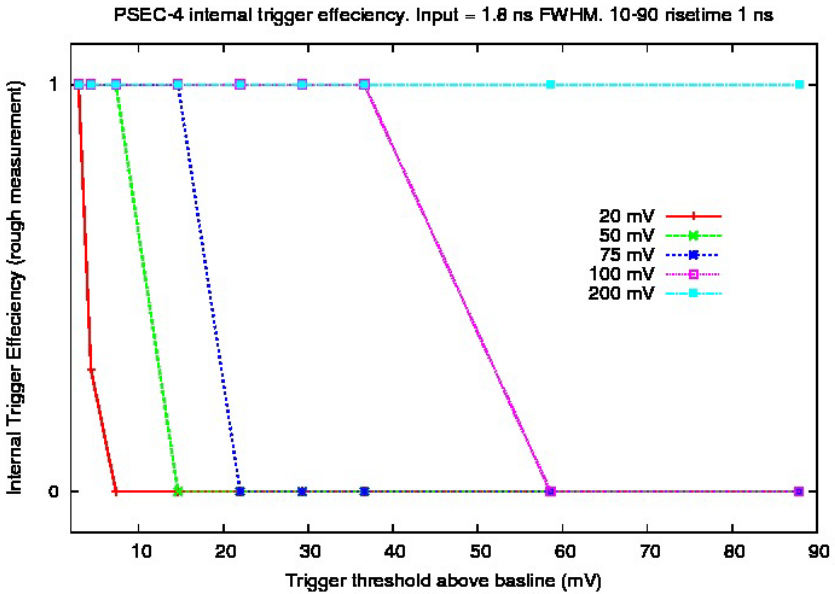
PSEC-4 Performance



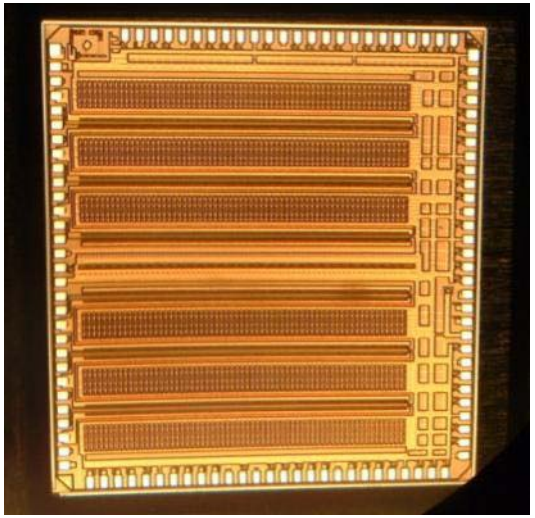
<noise> ~ 0.8 mV RMS



Self-triggering



Oscilloscope on a Chip?



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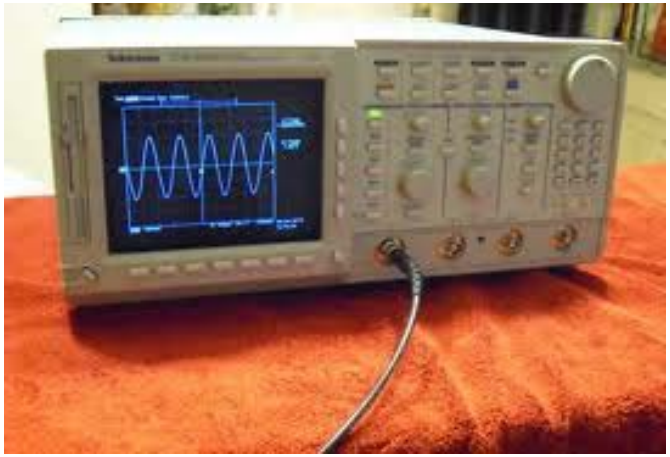
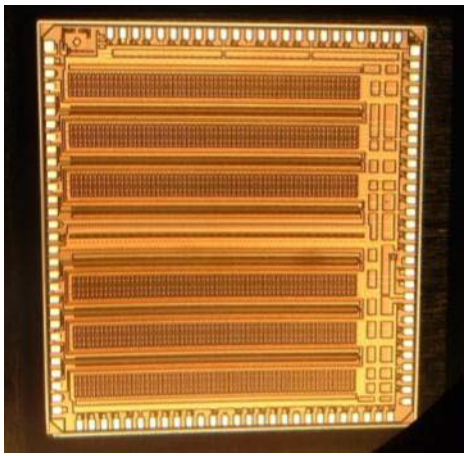


Oscilloscope on a Chip?

Not quite…a modified approximation:



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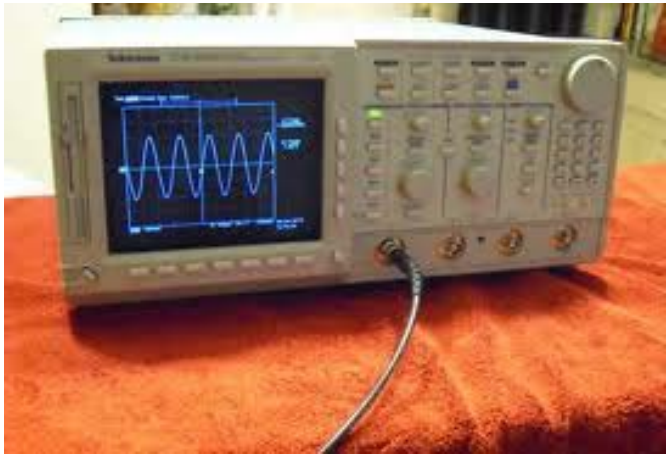
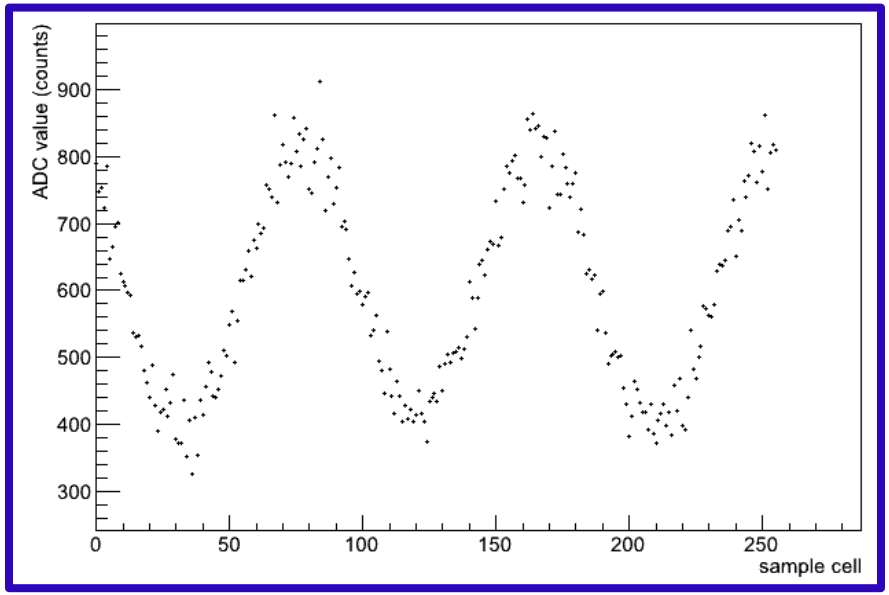


For example, a raw **PSEC-3** readout (10 GS/s) of 120 MHz, 150 mV_{rms} sine wave:



Kurtis Nishimura will discuss calibration

Summary

- PSEC4 a very nice SCA ASIC
- Competitive timing performance
- Storage depth a bit short → portfolio of ASIC options (next presentation)
- Gaining experience using in the lab
- PSEC5 (?) [discuss later]