Tile Calorimeter Upgrades

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Topics

- Overall ATLAS Upgrade Planning
- TileCal Upgrade
- Argonne Work on TileCal Upgrade
  - Front Ends
  - Power Supplies
- What happens when?
- Summary

ATLAS Upgrade Plans

- Goals
  - Accommodate and take advantage of higher luminosity
    - Average at least 3 x 10^{34} cm^{-2} sec^{-1}
  - Sufficient radiation tolerance
  - Replace radiation damaged systems
  - Increase capability
    - Add “staged” parts of systems, *e.g.*, layers of forward muon system
    - Improve performance and trigger sophistication
      - Modern electronics components
      - Replace some sensor systems: Tracker => all silicon

ATLAS/LHC Timeline

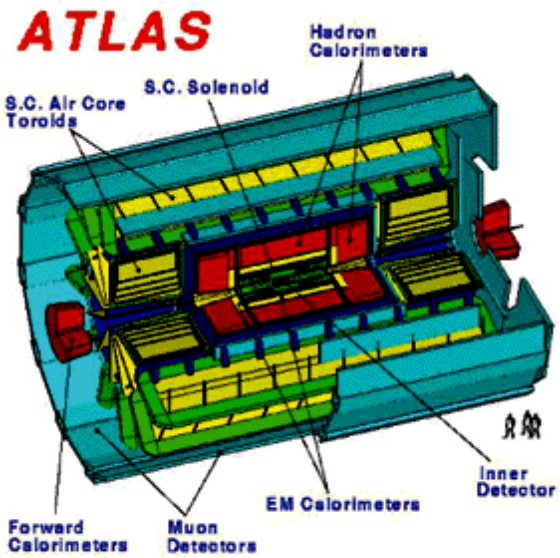
- January 2013
  - 15-24 month shutdown
    - Repair superconducting splices in LHC
    - Magnet repairs
    - General maintenance and system upgrades
  - ATLAS Maintenance
    - LAr LVPS
    - Tile LVPS
    - Install Insertable B Layer of Si tracking
- January 2017 (probably 2018)
  - ~18 month shutdown
  - ATLAS Phase I Upgrades
    - FTK
    - Forward muon detector and small wheels
    - L1 Calo upgrades
    - Under Consideration
      - Pixel replacement
      - First step in Calorimeter Readout (LAr, Tile)
    - Final scope to be recommended by current Phase I Task Force

ATLAS/LHC Timeline

- January 2021 (probably 2022)
  - 18-24 month shutdown
    - New tracking system
    - Complete calorimeter electronics
    - TDAQ Upgrades

- R&D is required for much of the work planned for 2017-18 and 2021-22
  - US ATLAS Operations Program
    - Reduced by reductions for DOE Collider R&D Program
  - DOE Collider R&D Program
  - NSF Cooperative Agreement

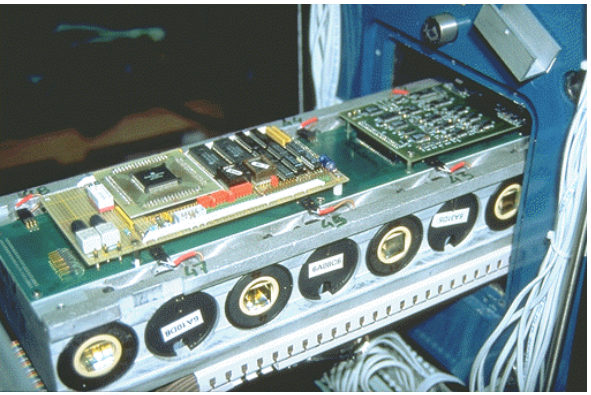
TileCal Upgrade Plan

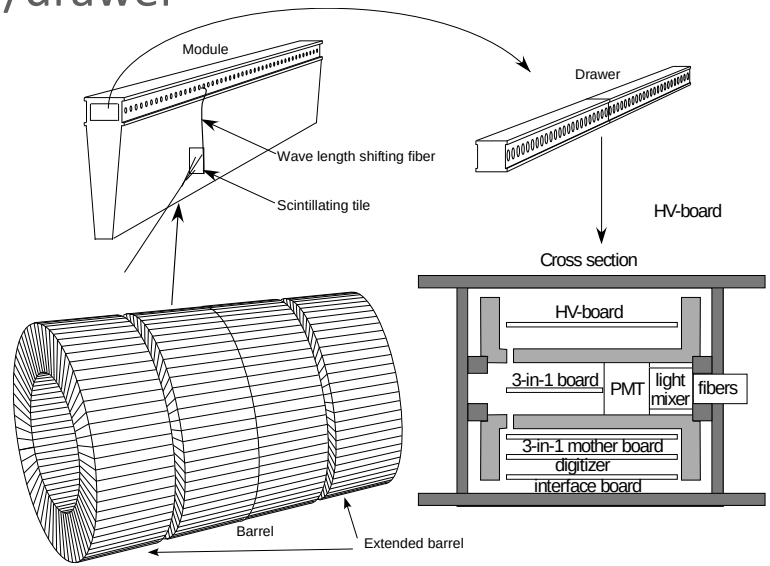


The present TileCal system

A TileCal drawer contains up to 48 PMT

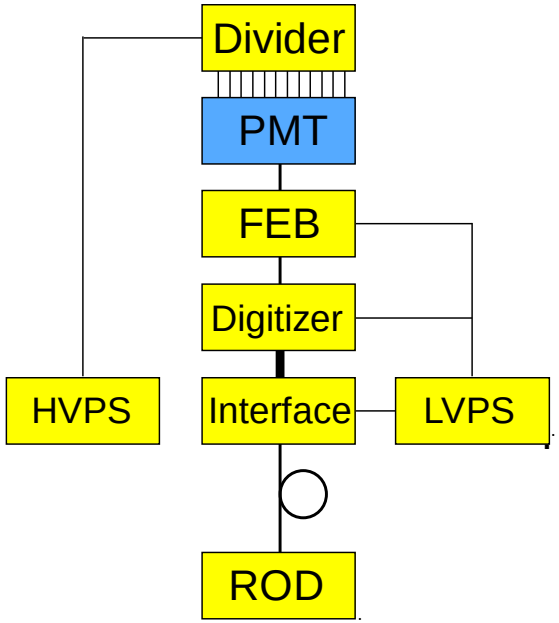
- Their signals are digitized and stored in a pipeline
- The signals are also combined into tower sums for transfer off the detector via analog trigger cables
- L1a selects sampled pulses for readout to off-detector RODs -1 fiber/drawer





Overall TileCal Upgrade Plan

- Replace virtually all electronics
  - Update aging components
  - Provide additional information to L1Calo to keep L1 rate below 100 kHz → FULL READOUT OF ALL TILE DATA
  - Ensure radiation hardness for up to 10 years at average 3 x 10^{34} $cm^{-2}sec^{-1}$
- Sub-projects
  - Low Voltage Power Supplies
  - Front ends
  - Digitizers
  - Buffering/derandomization
  - Optical transmission and reception
  - Trigger/data pre-processor
  - RODs



Argonne Involvement

- Overall Leadership
  - Gary Drake has provided specifications and vision for a new integrated TileCal readout system
  - L. Price is on the 4-member Upgrade Steering Group
    - Restarted TileCal upgrade planning in 2008
- Front Ends
- Digitizers
- Low Voltage Power Supplies
- Test beams

***E.g.*, QIE**

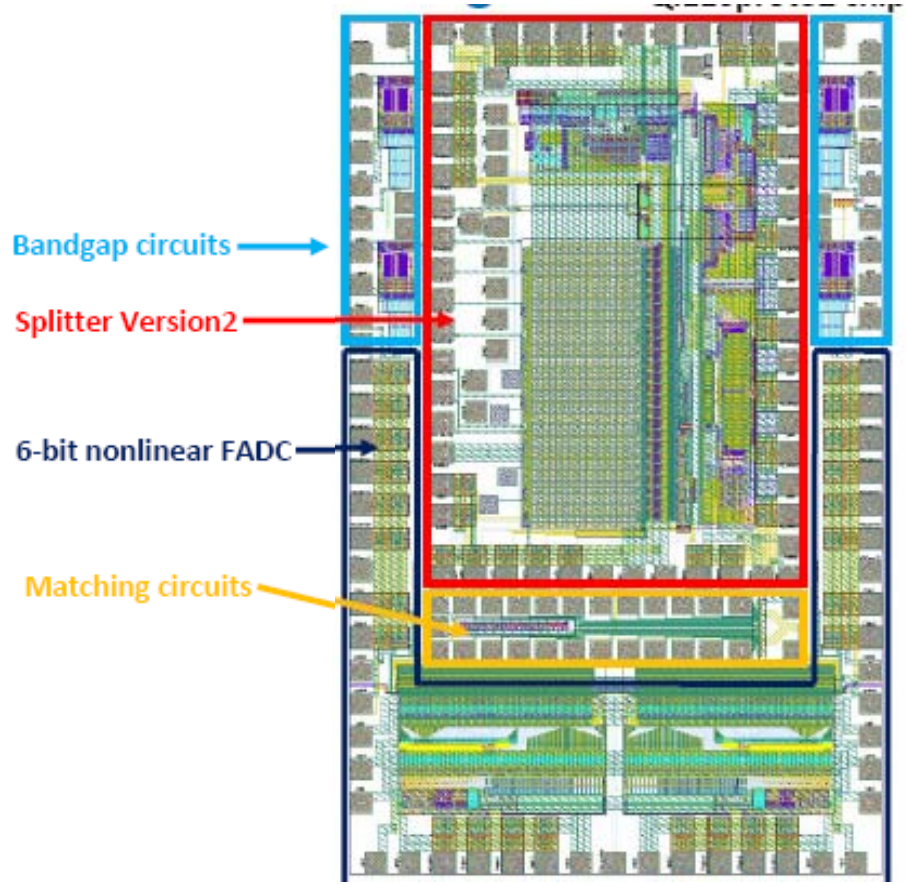
QIE ASIC for Tile Front-End

- We have proposed to develop a new version of the Fermilab QIE ASIC to provide
  - Very low noise (<24 fC) amplification
  - Digitization linear to <1 lsb with 16 bits dynamic range
  - Timing (completely new feature in QIE) to 1 nsec
  - Charge injection for calibration (0.5% uniformity; 0.1% repeatability)
  - Integrator for calibration with source (0.2% uniformity)
- General Features of QIE Family
  - 50 ohm input, nearly constant over dynamic range
  - No pulse shaping; deadtimeless digitization
  - Pipelined operation

QIE7B for MINOS

QIE ASIC for Tile Front-End

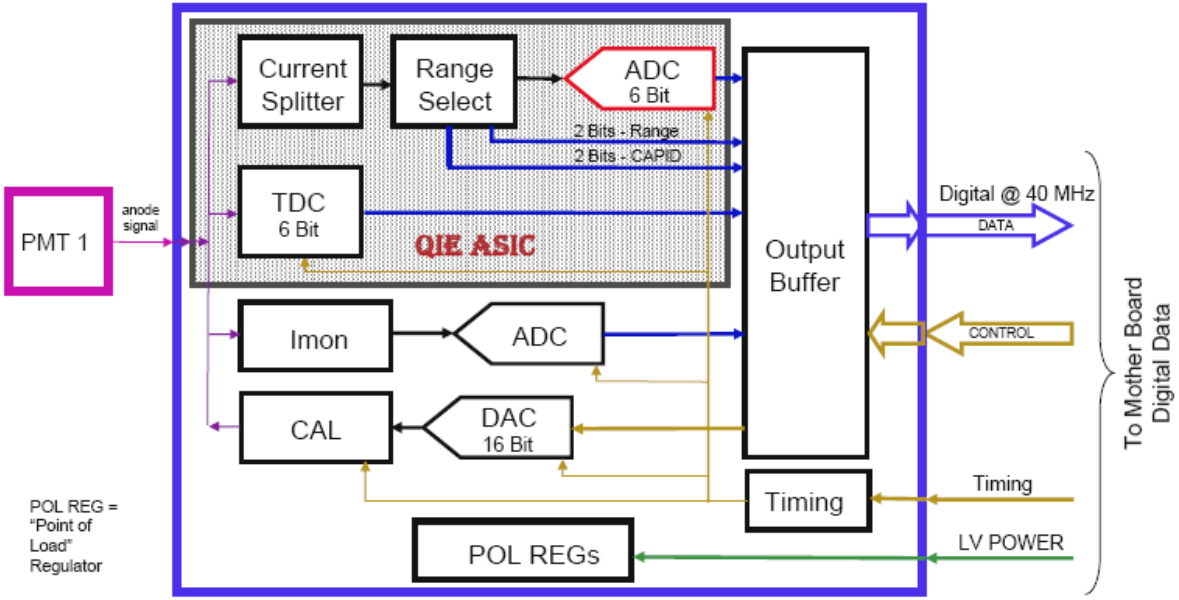
- Status of QIE10 design
  - 2 test chips produced so far
    - Submissions Feb 22 '10 and Aug 30 '10
      - Fabricated through MOSIS AMS 0.35u SiGe BiCMOS process
    - Both received and tested
      - Most circuits work as expected
      - Minor problems found and understood
    - Radiation tests
      - Gammas, Neutrons, Protons
        - » Successful so far



QIE: Argonne's Role

- QIE10 is a joint development with FNAL, which has the ASIC design capability
  - Tom Zimmerman
- Argonne is doing
  - Specification for TileCal
  - Interacting with and evaluating design and simulations
  - Bench testing and critique for iteration
  - Radiation Testing
  - Integration into TileCal readout system

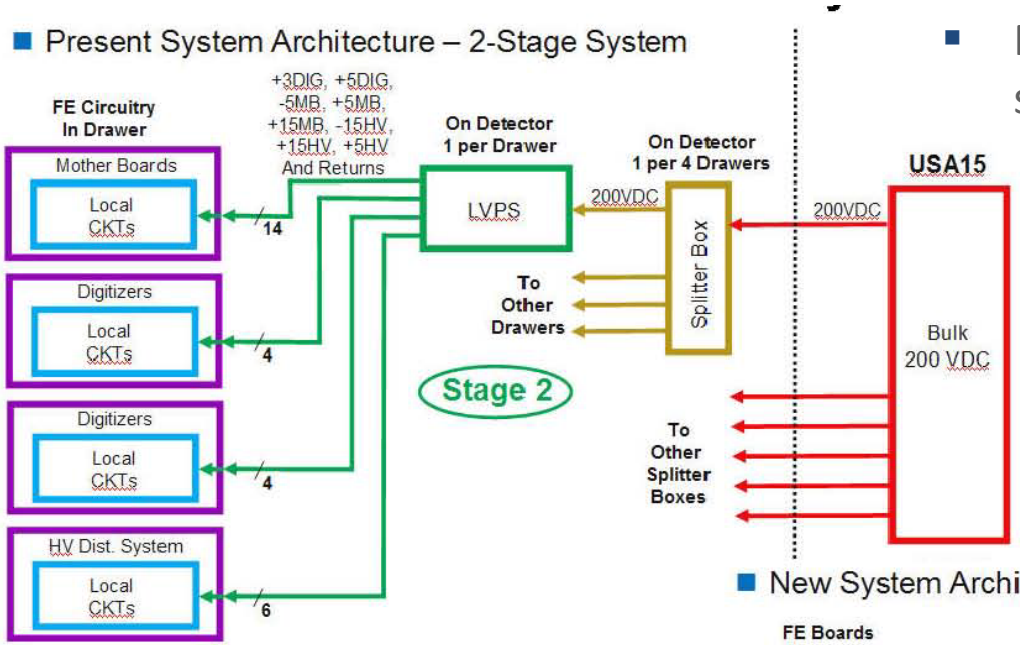
A Conceptual Design of the QIE Front End Board



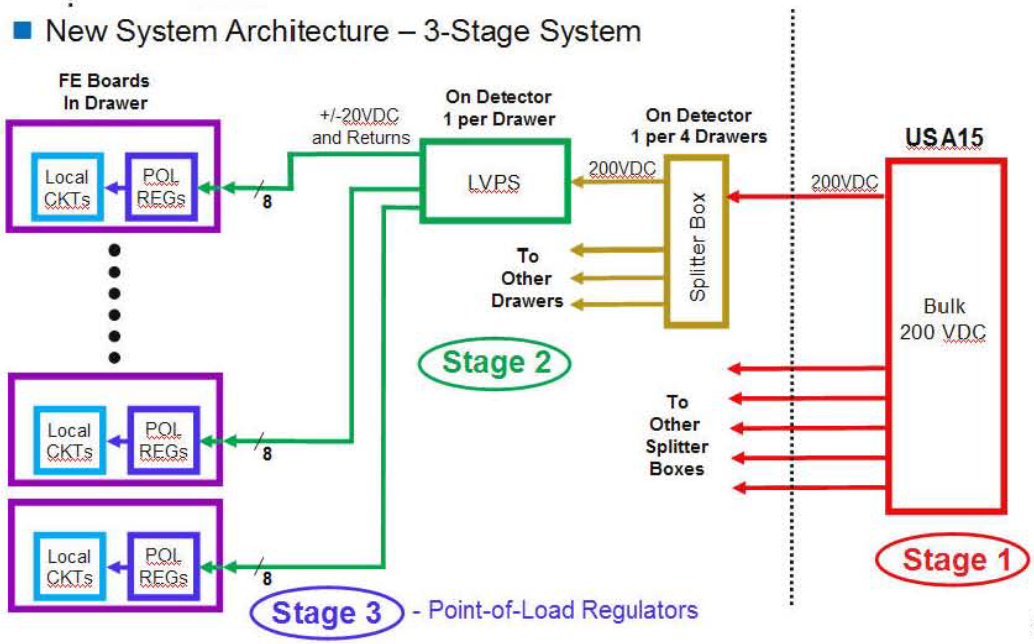
Very approximate schedule for QIE development

- First pass submission of “full” design: August 2011
- Receive chips: Jan 1 2012
- Bench testing: Jan-June 2012
- 2nd submission: July 2012
- Bench testing: October 2012 – March 2013
- Develop interface and instrumentation for beam test: 2013-4
- 2015: Test beam (~10 channels)
- 2018 (?): Phase 1 shutdown
  - Install (small?) fraction of new system

TileCal LVPS Upgrade



- Move from 2-stage architecture to 3-stage power architecture
  - Only 2 voltages from LVPS box (instead of 8)
  - 3rd stage is local point-of-load regulators at multiple points in readout drawer
  - Add redundancy with multiple bricks for each voltage in LVPS box

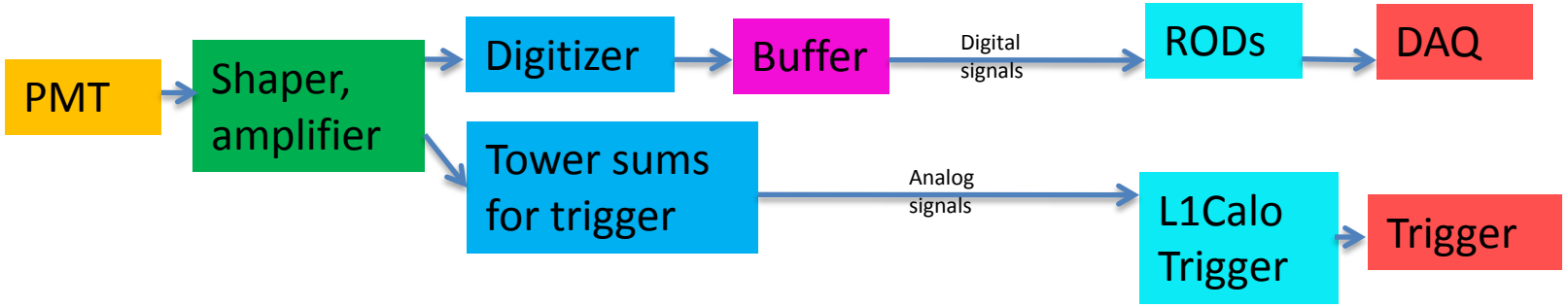


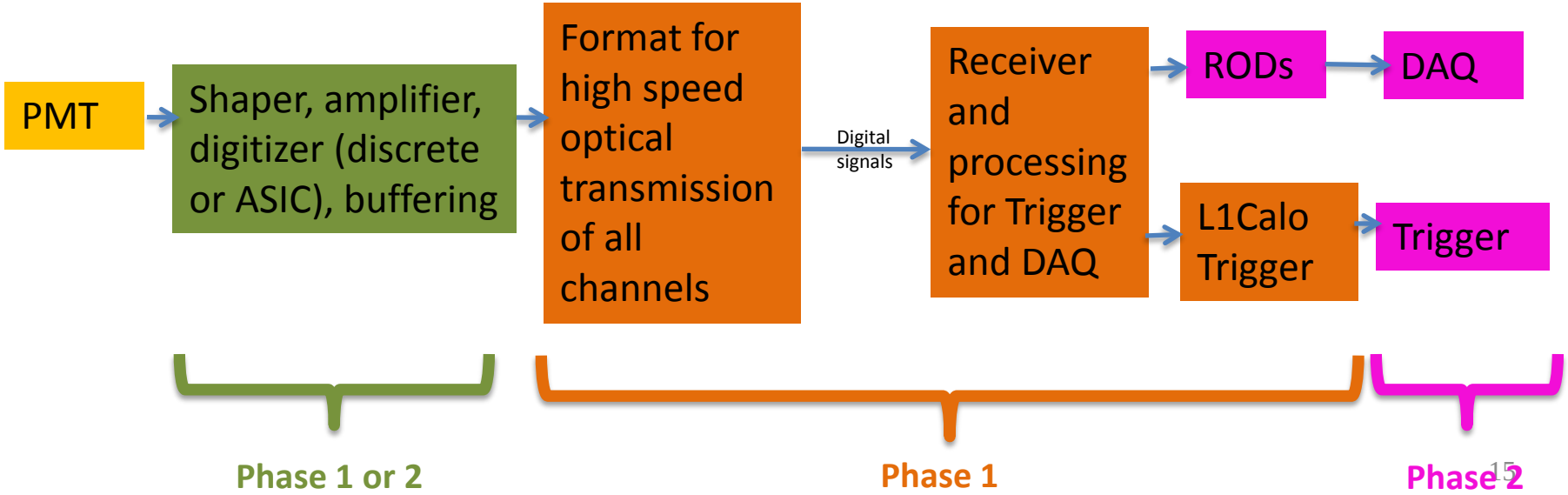
- **Main issues to be addressed**
  - Voltages and currents required
  - Choice of POL regulators
    - **Test CERN design**
    - **Address negative voltages**
  - Component design and radiation testing
  - Choose connectors wisely!

What happens when?

- Fast moving target! Suggestion for a phased approach
- Currently:
  - Analog Trigger tower signals are formed on-detector and transmitted to the trigger cavern, where the summed signals are digitized and processed to form a L1-decision.
  - Front-End digitized pipelined analog samples read out only upon arrival of a L1-accept signal from the central trigger processor
- Phase-0 (2012-2014)
  - A few tower sums will be replaced by dual boards, where in addition to the analog trigger towers, individual layers will be digitized and transmitted over fast optical links.
  - In the counting room, a new processor will process the digitized layer information, extract trigger primitives which will be sent to the L1 processors.
  - This demonstrator would be used initially for standalone monitoring and analysis to validate the architecture
  - Install for a trigger partition for LAr and 1 or 2 drawers for TileCal
- Phase-I (2014-2018)
  - The L1-trigger processors potentially will use only the layer digitized information
  - Extend the dual trigger signals upgrade to the full calorimeter (~20k LAr +20k Tile in total)
- Phase-II (2017-2022)
  - All the Front-End electronics will be upgraded with more radiation tolerant electronics with an architecture similar to what was proposed earlier for the TBB upgrade
  - Also the main RODs boards will be upgraded with the same or similar technology as the TTRODs (firmware changes)
- Or…
  - Install whole TileCal upgrade in 2018
  - Needs clarification and decision urgently!
    - Phase 1 Task force reports during the summer

Phasing of TileCal Upgrade





Summary

- LHC and ATLAS Upgrade Schedules are evolving in real time
  - Expect shutdowns of > 1 year in 2013, 2018, and 2022
  - Argonne has provided overall leadership for upgrade planning
  - …and is working specifically on front-end electronics and low voltage power supplies
    - QIE option for signal processing and digitization
    - Power supplies with 2 voltages, POL regulators, and redundancy
  - We are doing R&D, but need explicit funding
    - Part of US ATLAS proposal to DOE collider R&D
    - US ATLAS Operations Program