FTK Status

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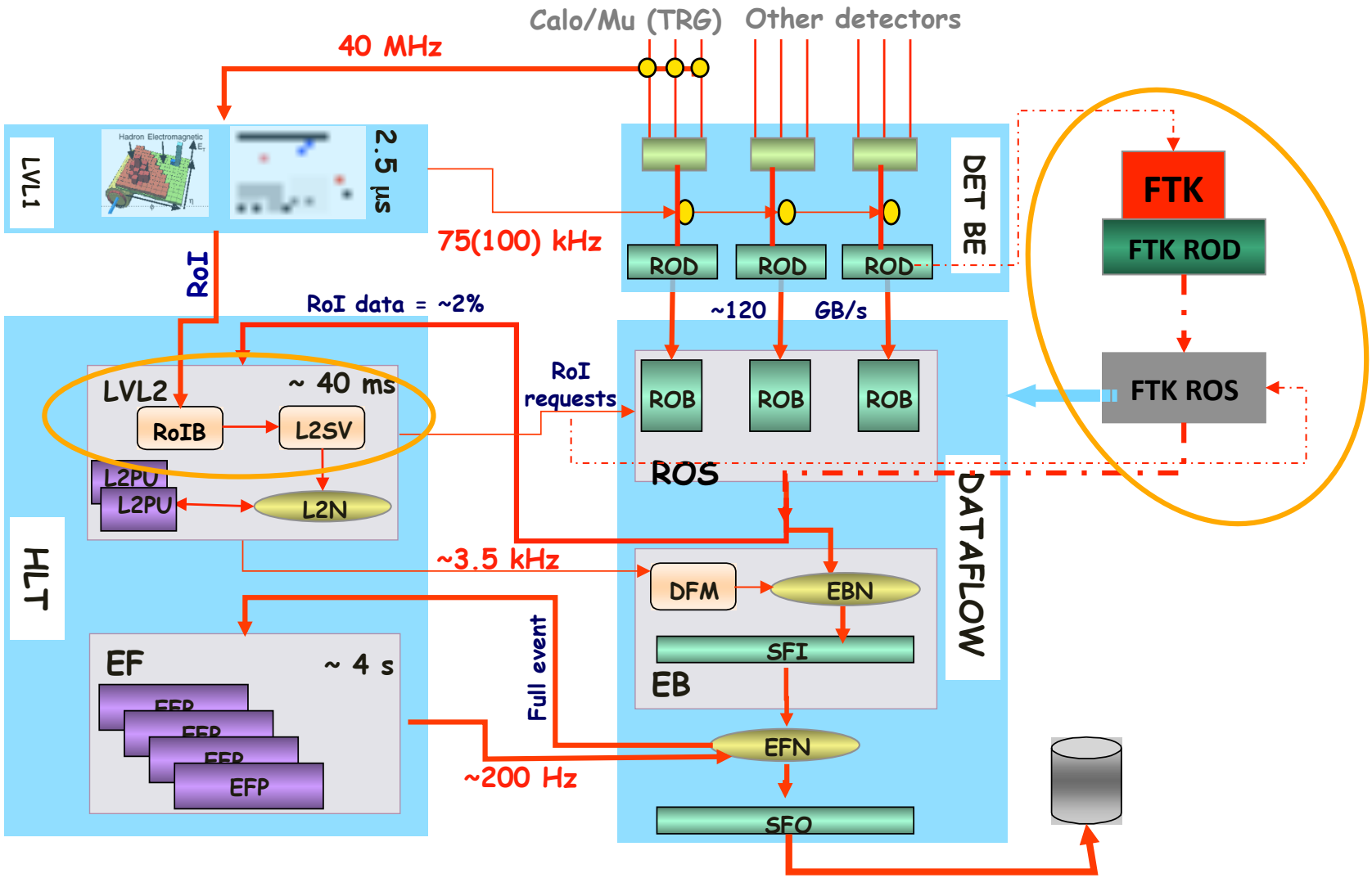
Outline

- Fast TracKer (FTK) System overview
- ANL commitment
  - Work done before the initial design review
  - Work ongoing till TDR
  - Long term plan

FTK in Brief

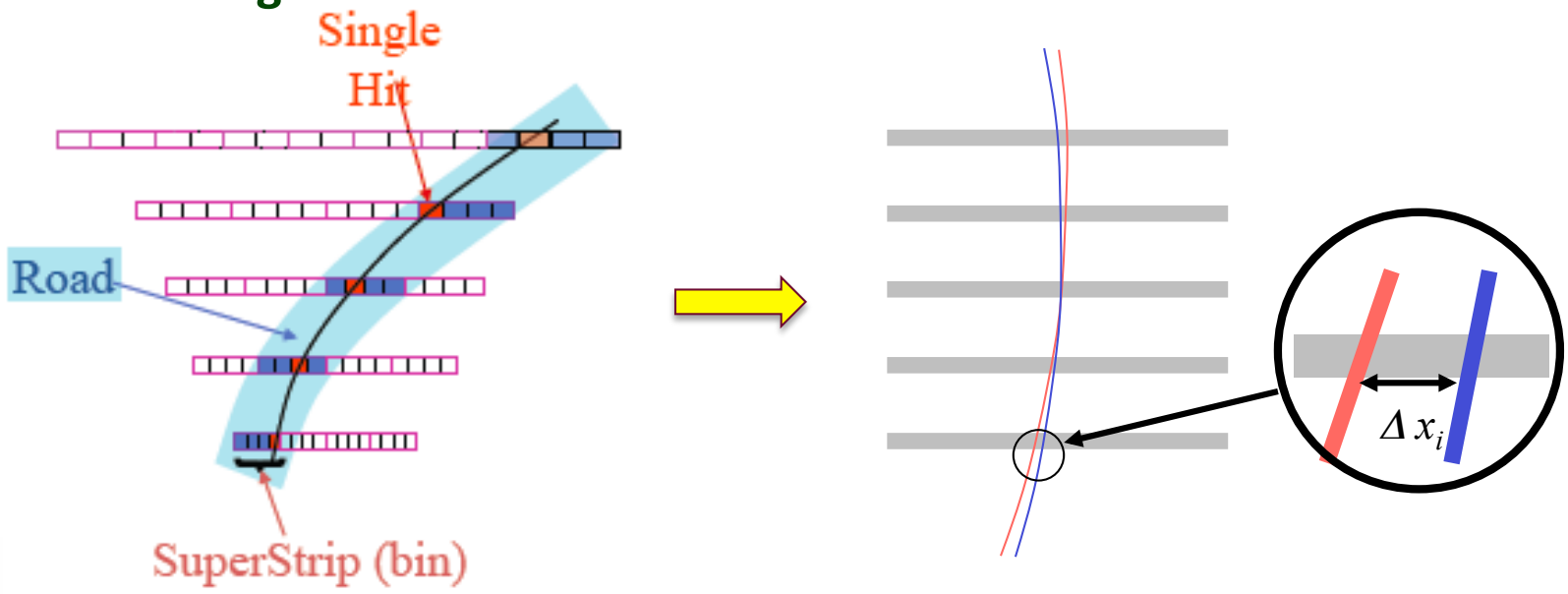
- A hardware track finder
  - Completing global tracking at the beginning of Level-2 trigger
  - Enhancing the capability for b tagging, τ tagging and lepton isolation
- Project timeline
  - R&D proposal in 03/2008
  - Technical Proposal (TP) in 01/2010
  - Initial design review in 12/2010
  - EB approval in 12/2010
  - CB approval in 06/2011
  - TDR in earlier 2013

ATLAS TDAQ+FTK



FTK Approach

Use hardware to perform the global tracking in two steps pattern recognition and track fit



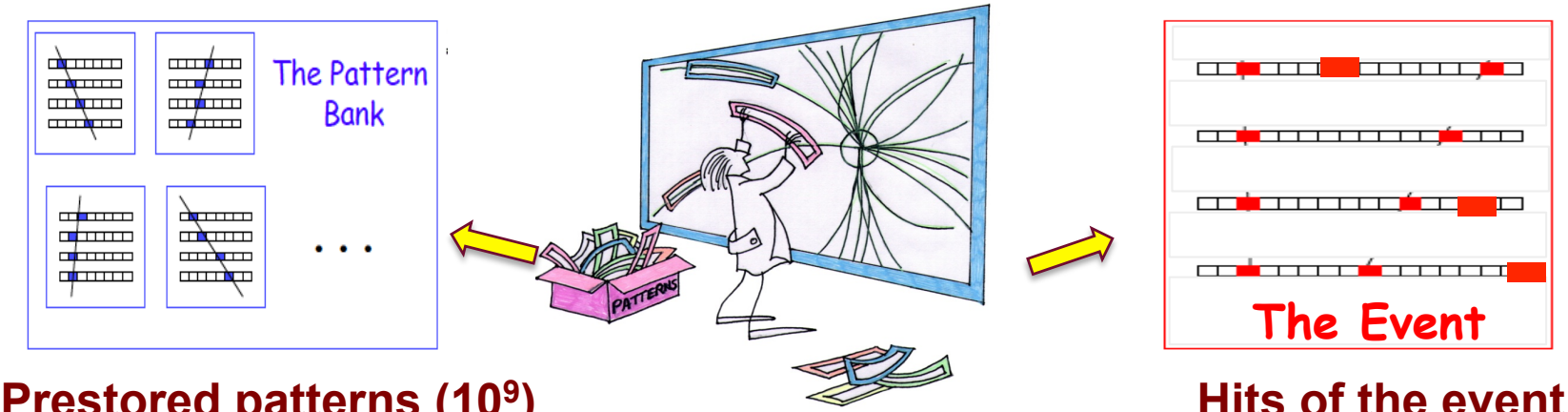
Pattern recognition in coarse resolution (superstrip➔road)

Track fit in full resolution (hits in a road)

$$F(x_1, x_2, x_3, \ldots) \sim a_0 + a_1\Delta x_1 + a_2\Delta x_2 + a_3\Delta x_3 + \ldots = 0$$

Road size to balance the workload between two steps

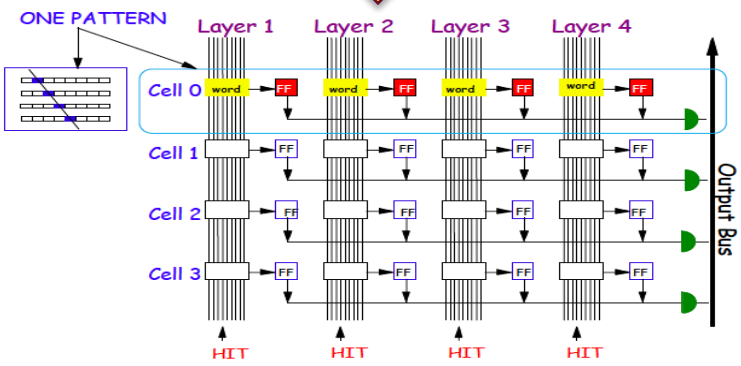
Pattern Recognition



Prestored patterns (10^9)

Hits of the event

Content-addressable Memory (CAM)



Fast pattern recognition

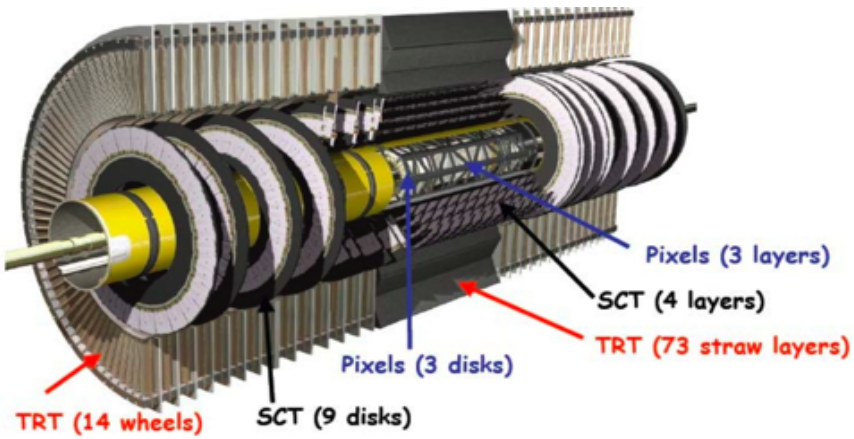
Track Fitting

- Determine the helix parameters and χ^2
- Fit with the local silicon hit coordinates (one module in each layer) in linear

$$p_i = \sum_{j=1}^{14} a_{ij} x_j + b_i$$

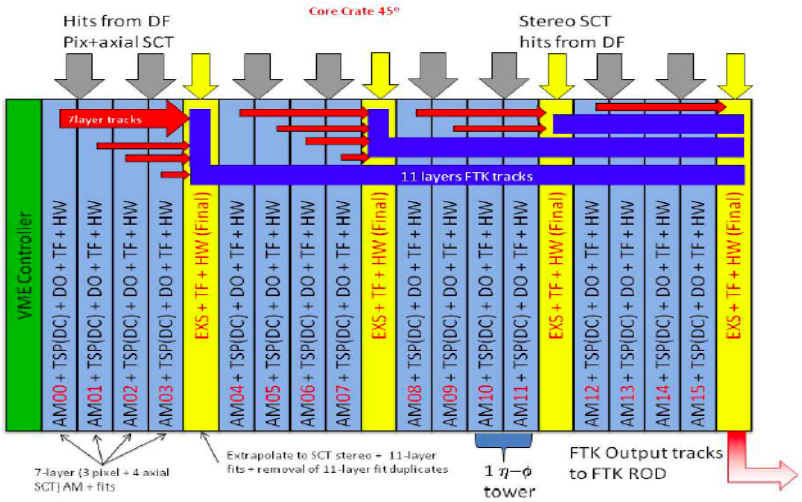
  - P_i: the helix parameters and χ^2 components
  - X_j: the hit coordinates in the silicon layers
  - a_{ij} & b_i: prestored constants determined from full simulation or real data track
- Very fast in DSPs (~1 ns per track)

System Overview

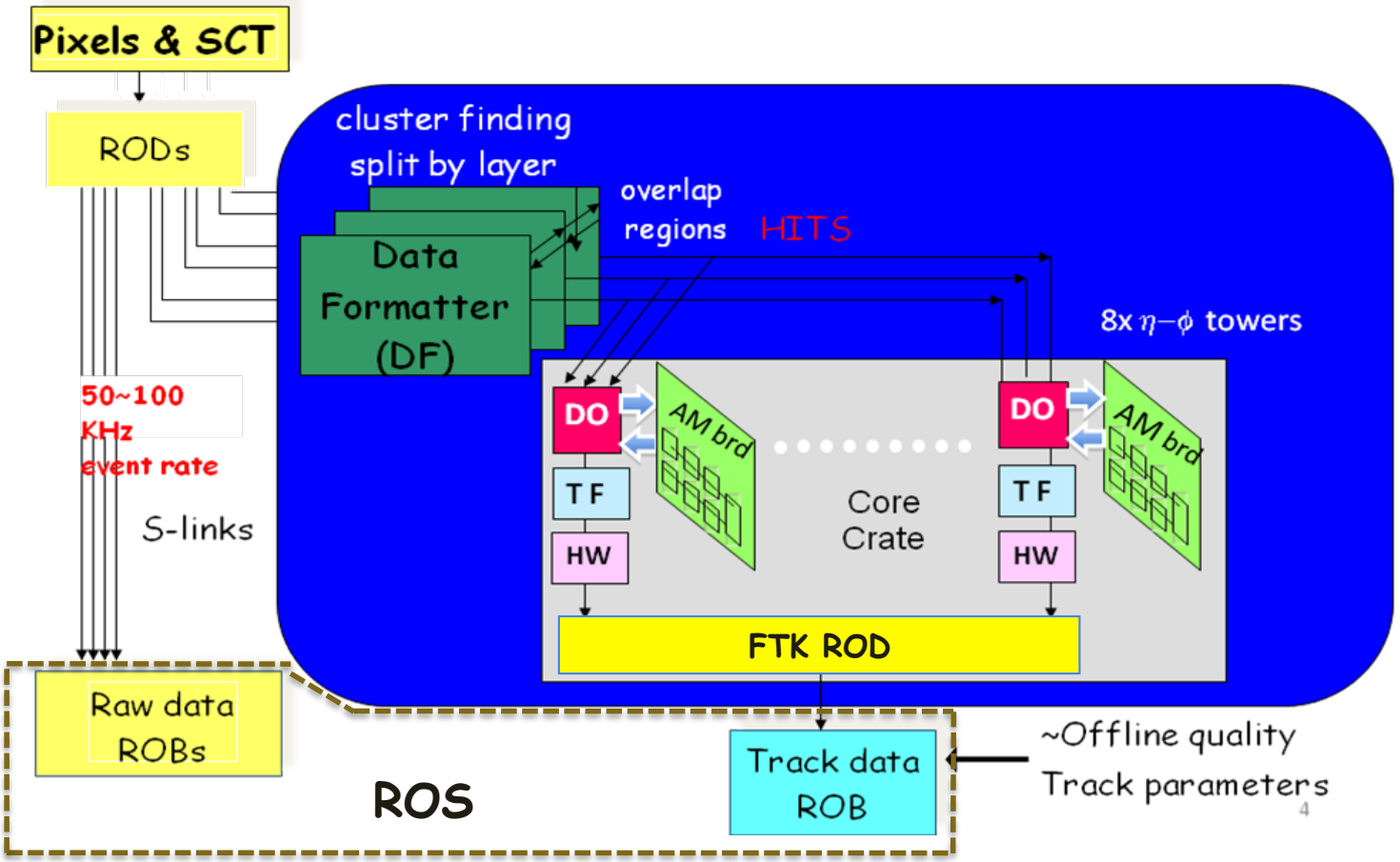


- PIX (3 layers) & SCT (4 double layers)
- Architecture of 11 layers in one step (PIX 3 + SCT 4 axial + SCT 4 stereo) unaffordable
- Two stage plan:
  - PIX 3 (&IBL)+SCT 4 axial, plus one more layer to be chosen
  - SCT stereo layer extrapolation & 11-layer fit

- Each core crate with 1/8 azimuthal coverage
- 4X2 η−ϕ towers in each core crate, each tower with two processing units
- Overlaps to maintain high efficiency



System Functional Sketch



Interface to the Current System

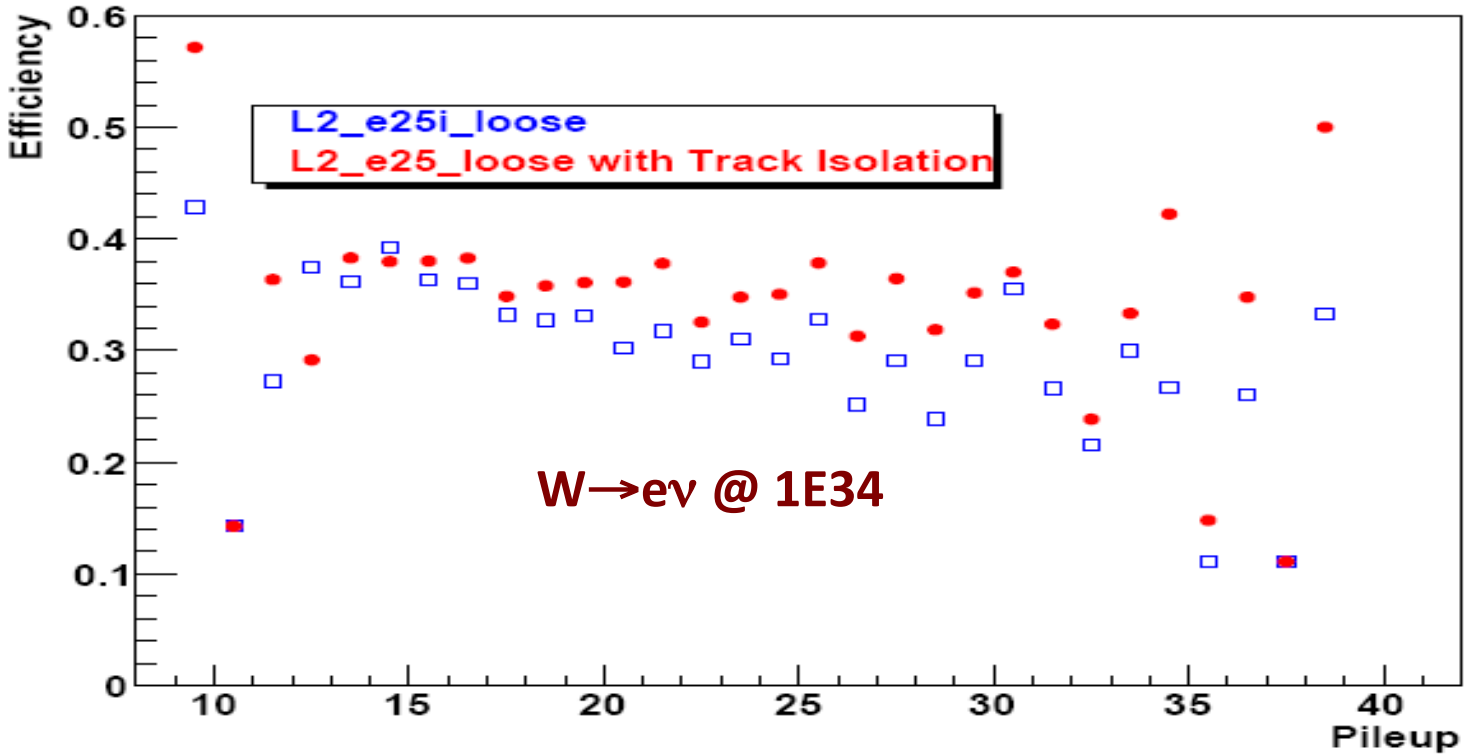
- **Input (receiving data from the detector Readout Drivers (ROD))**
  - **Dual output interface card needed in the detector RODs**
- **Output (sending data to the Level 2 trigger (LVL2) via dataflow system)**
  - **Readout System (ROS): Special configuration or special running mode or different hardware components are being investigated**
    - **The output event size for all tracks with PT > 1 GeV/c at 3×10^{34} could reach 20 kB or more.**
  - **Dataflow: Event format, fragment decoder, network traffic handling, etc**
  - **High Level Trigger (HLT): FTK track based algorithms could be plugged in the trigger configuration**

ANL Commitment

- Who are working on the project
  - Scientists: Blair, Blazey (ANL/NIU), Proudfoot, Zhang
  - HEP engineer group: Anderson, Drake, Kreps
  - A postdoc to be hired
- What we are working on
  - Work done before the initial design review
  - Work ongoing till TDR
  - Long term plan

Electron Isolation

- Electron isolation in LVL2 inherited from the Level-1 calorimeter trigger
- Calorimeter based electron isolation may degrade with high pileups at high luminosity
- Offline-like tracks of the full event available at the beginning of LVL2 from FTK
- The effectiveness of track isolation on top of current LVL2 being investigated



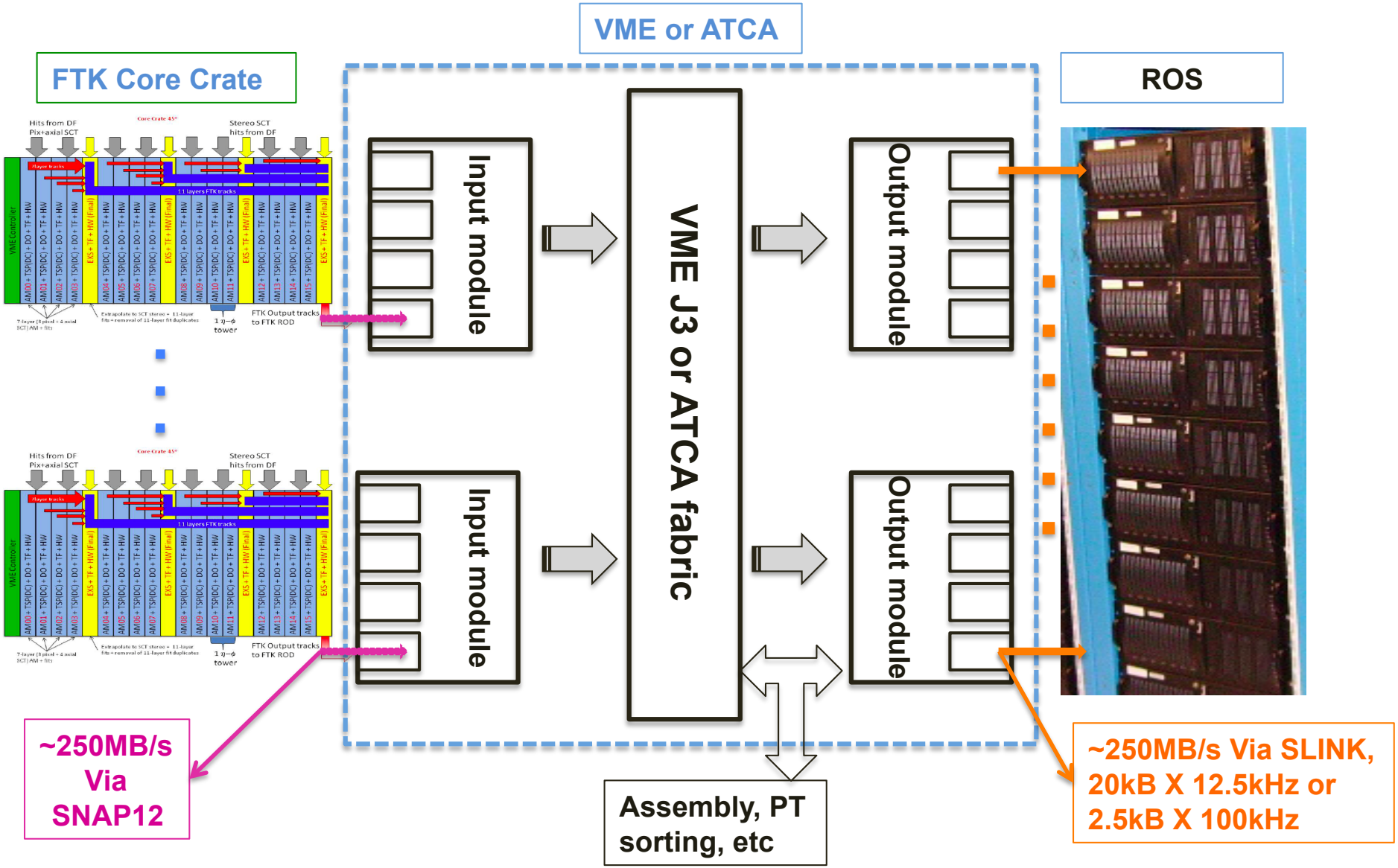
FTK-Dataflow Communication Challenge

- FTK data to be used at full level 1 accept rate (100 kHz)
- Traffic to be introduced
  - ~4K Level 2 applications request data at 100 KHz
  - ~100 Event Building applications request data at 3.5 KHz
- ROS constraint
  - The typical data size of 1 KB from one input link
  - Maximum of 15 input links
  - Capable of ~20 kHz request rate
- Solutions
  - ROS with a special configuration: one input link only; each ROS seeing 100 kHz data
  - ROS in a special mode: 100 KHz/# ROS to each ROS based on L1ID; a given ROS seeing data of a fraction of all L1IDs
  - Each solution with pros & cons

Milestones to TDR

- Specification documents for boards: Spring, 2011
  - FTK-LVL2 interface (FTK ROD) from ANL
- Complete critical studies: Summer, 2011
- Dual-output HOLA production start: Summer, 2011
- AM chip submission: Autumn, 2011
- Vertical slice moves to CERN: Autumn, 2011
- Operate vertical slice with beam: Autumn, 2012
- Tested prototype boards: Autumn, 2012
  - FTK-LVL2 interface (FTK ROD) from ANL
- Complete TDR: Spring, 2013

FTK-LVL2 Interface Baseline Design



Long Term Plan

- FTK-LVL2 interface (FTK ROD) from design to operation
- FTK algorithms and integration into DAQ/HLT, FTK simulation and physics study with FTK data
- FTK testbed with full functionality at ANL
- Contribution on 3D chip R&D (collaborate with Fermilab)
- Testing, installation, commissioning and operation

HLT Integration & Algorithms

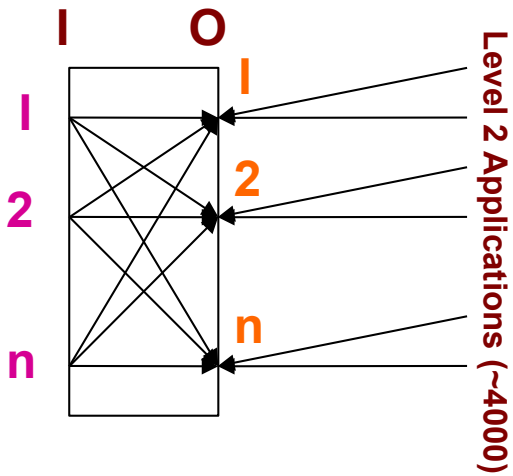
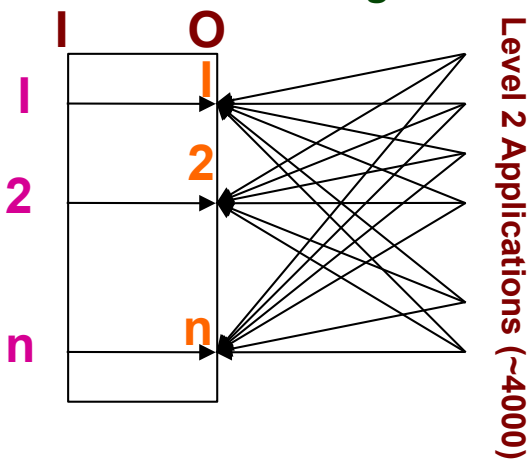
- **Implementing dataflow functionality and HLT configuration change to handle FTK data**
- **Developing FTK based algorithms in HLT to benefit**
  - ***b* tagging**
  - **τ trigger**
  - **Isolated muons**
  - **Isolated electrons – incl. balance between Level-1/HLT isolation**
  - **…**

Summary

- **Good progress on FTK and the group gearing up**

Comparison between Solutions

- **Pros**
  - Low request rate to ROS
  - More flexibilities to maneuver the data (Pt sorting, etc)
- **Cons**
  - More complex hardware
  - Potential large traffic per output link



- **Pros**
  - Hardware straightforward to expand
  - Partial data loss in case of problem
- **Cons**
  - High request rate to ROS
  - More work in LVL2
  - Potential more ROSs thus more network connections
  - Potential implication to the core crate in case of large traffic