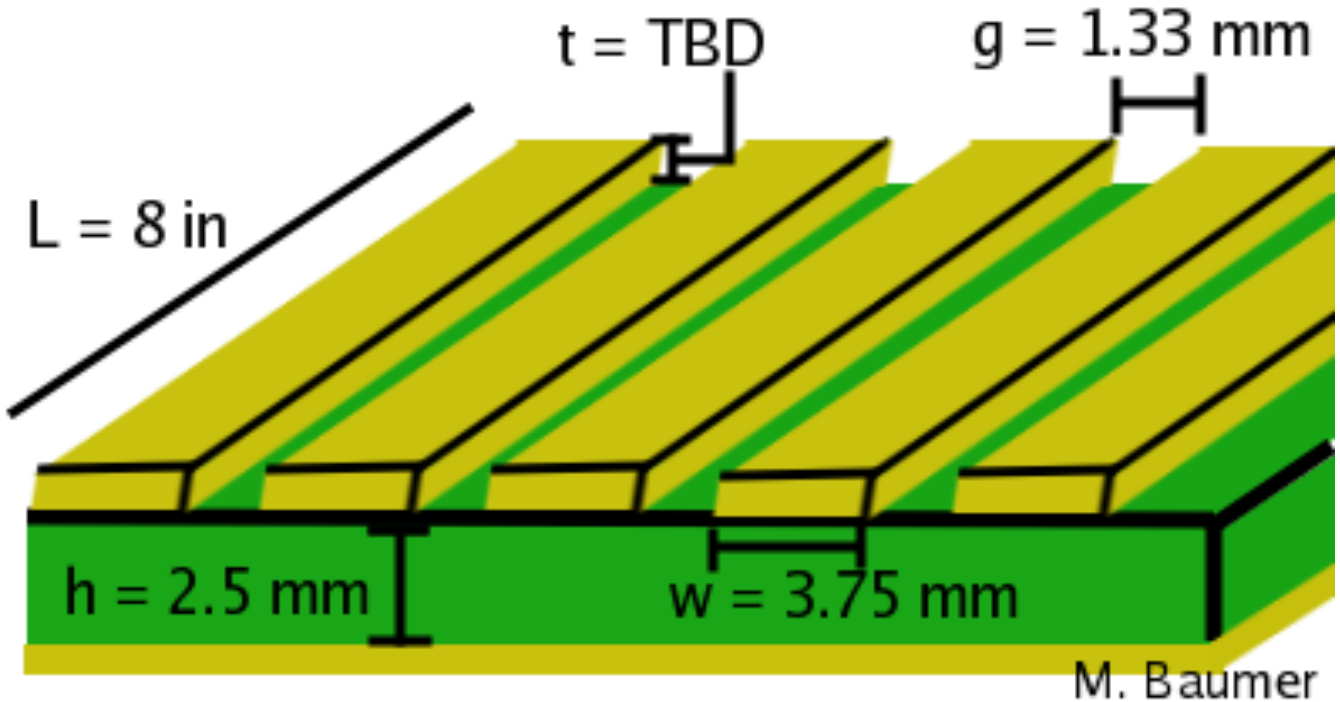
Anode Readouts

Michael Baumer and Zhongtian Dai
University of Chicago

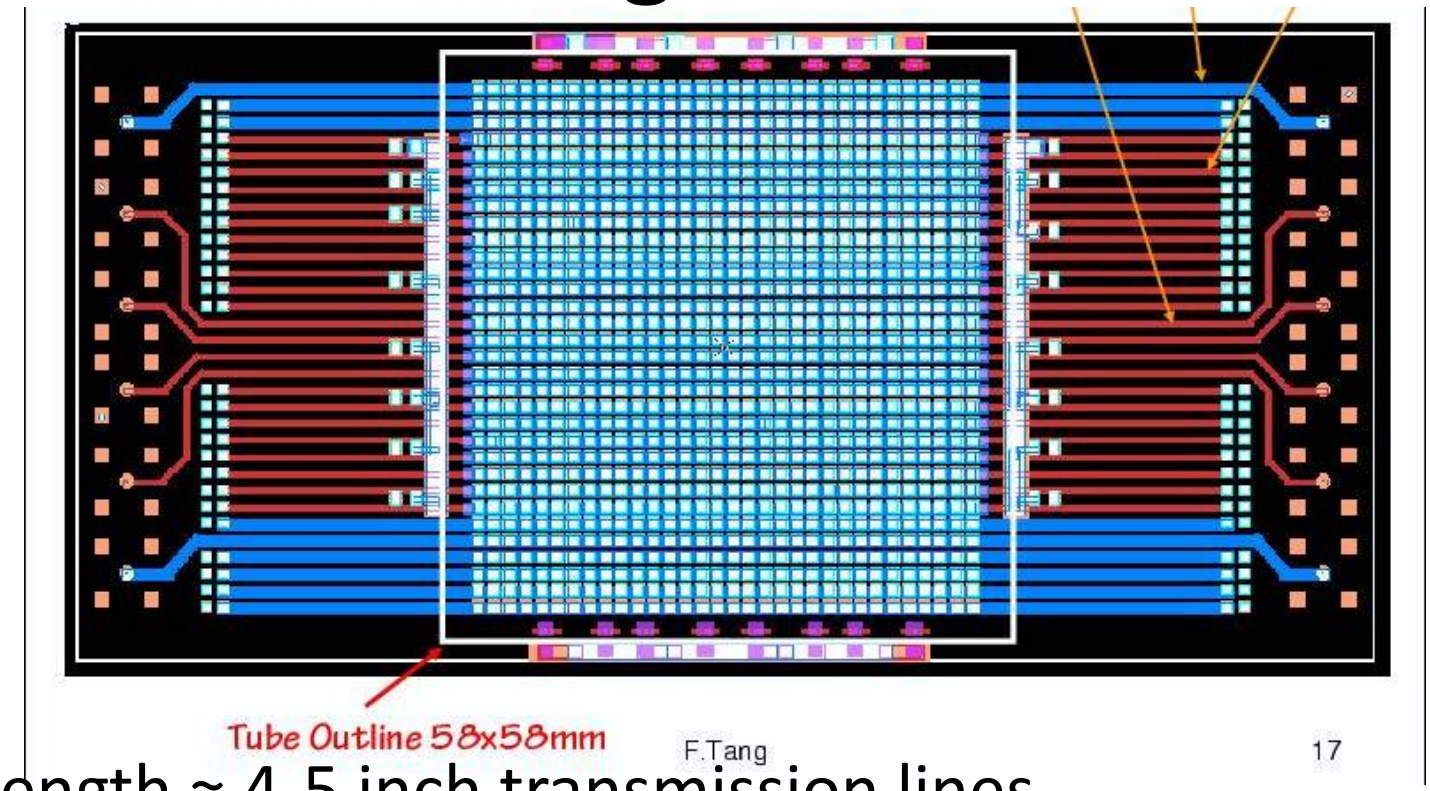
LAPD Collaboration Meeting, ANL, October 15-16, 2009

Geometry and Impedance



- Analytical approximation given in Gupta, et al. *Microstrip Lines and Slotlines*.
- Key parameters are ε, w/h, and gap width.

Fukun Tang's Anode Card



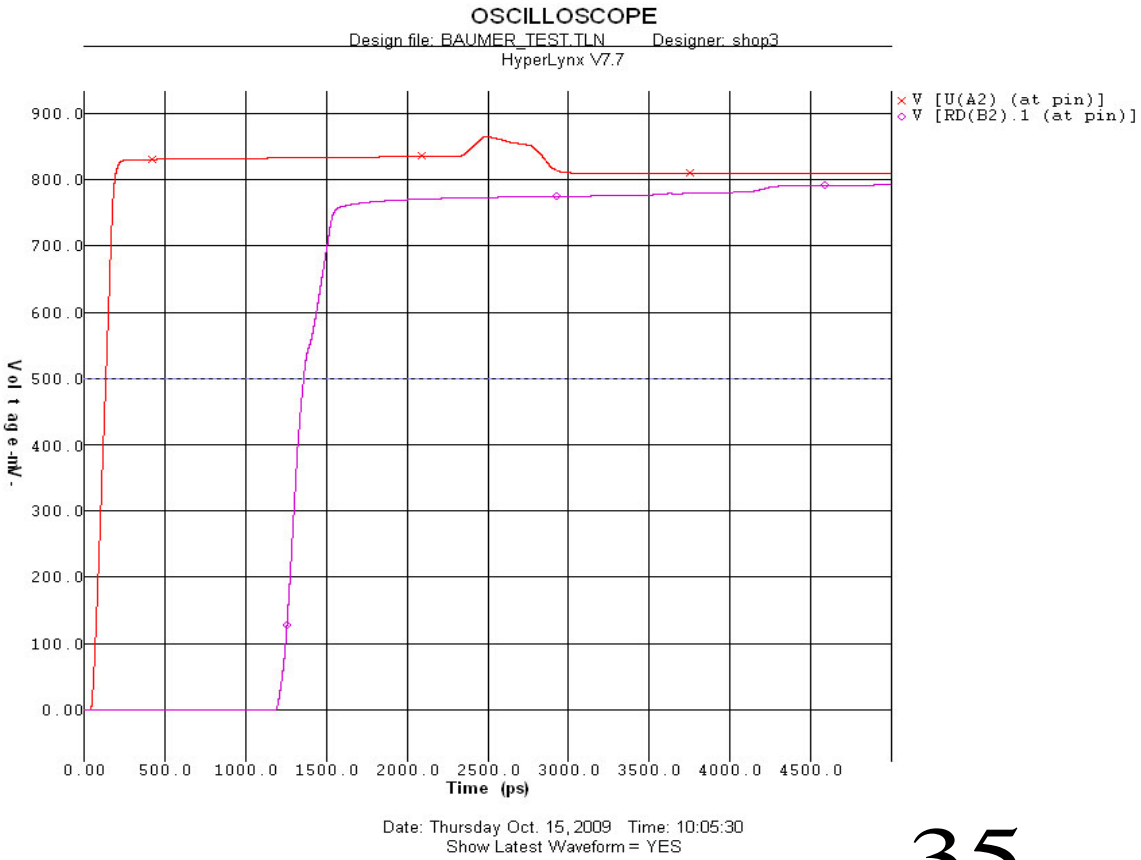
- Length ≈ 4-5 inch transmission lines
- Impedance = 50 Ω
- Simulated Bandwidth = 3.5 GHz
- Measured Bandwidth ≈ 3.5 GHz

Thickness = 540 µm

Anode Timing

- Pulse Sampling—Resolution depends on SNR
  - At low SNR (low PE), minimizing leading edge distortion becomes more important.
- Measure time at both ends of the lines to find the time of arrival and position.
- Leading edge contains most valuable timing information—must preserve as the signal propagates from inside the detector to the ASIC.

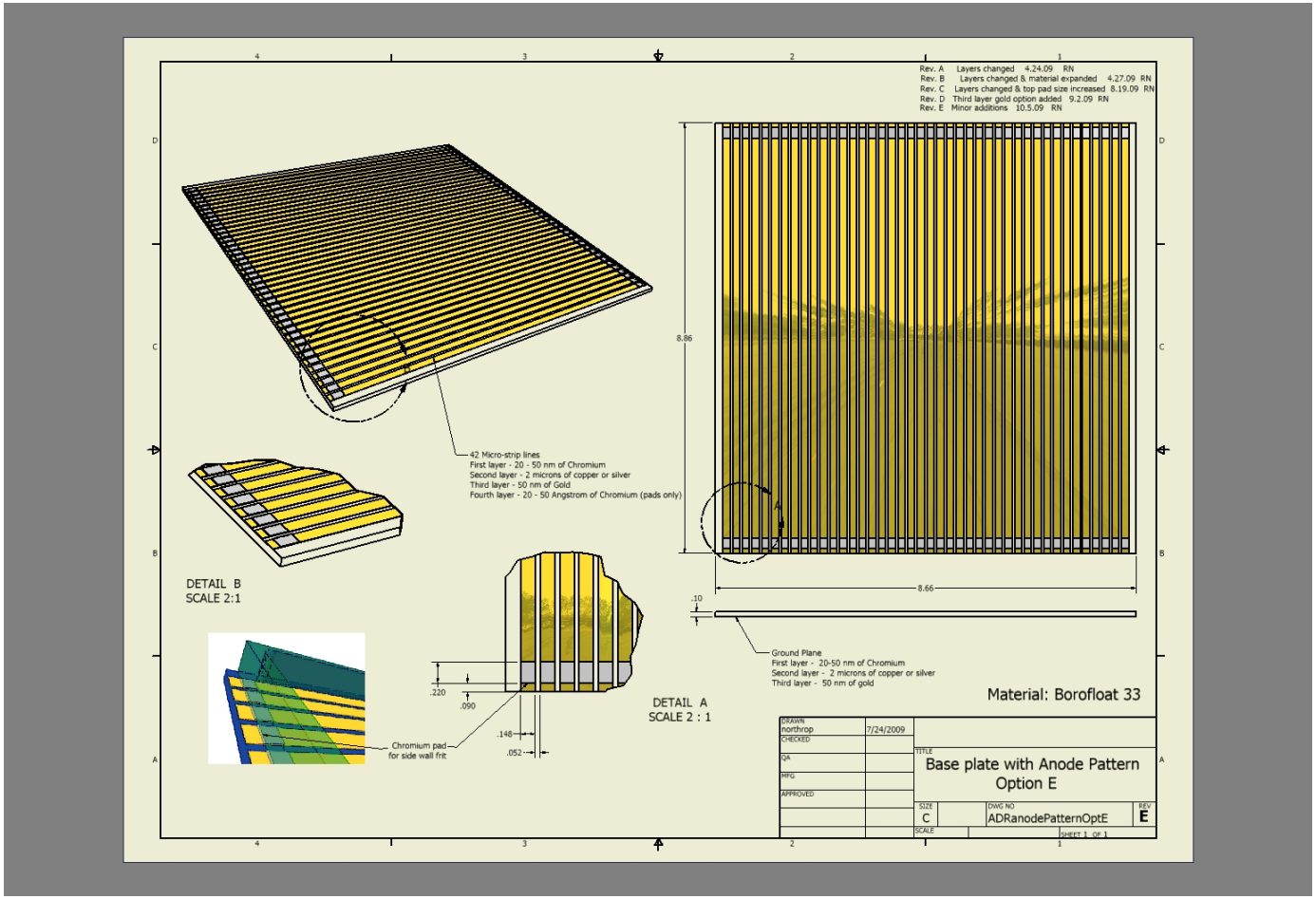
Motivation



$$BW = \frac{.35}{\sqrt{(\tau_{input})^2 - (\tau_{output})^2}}$$

Where τ denotes the risetime of the pulse.

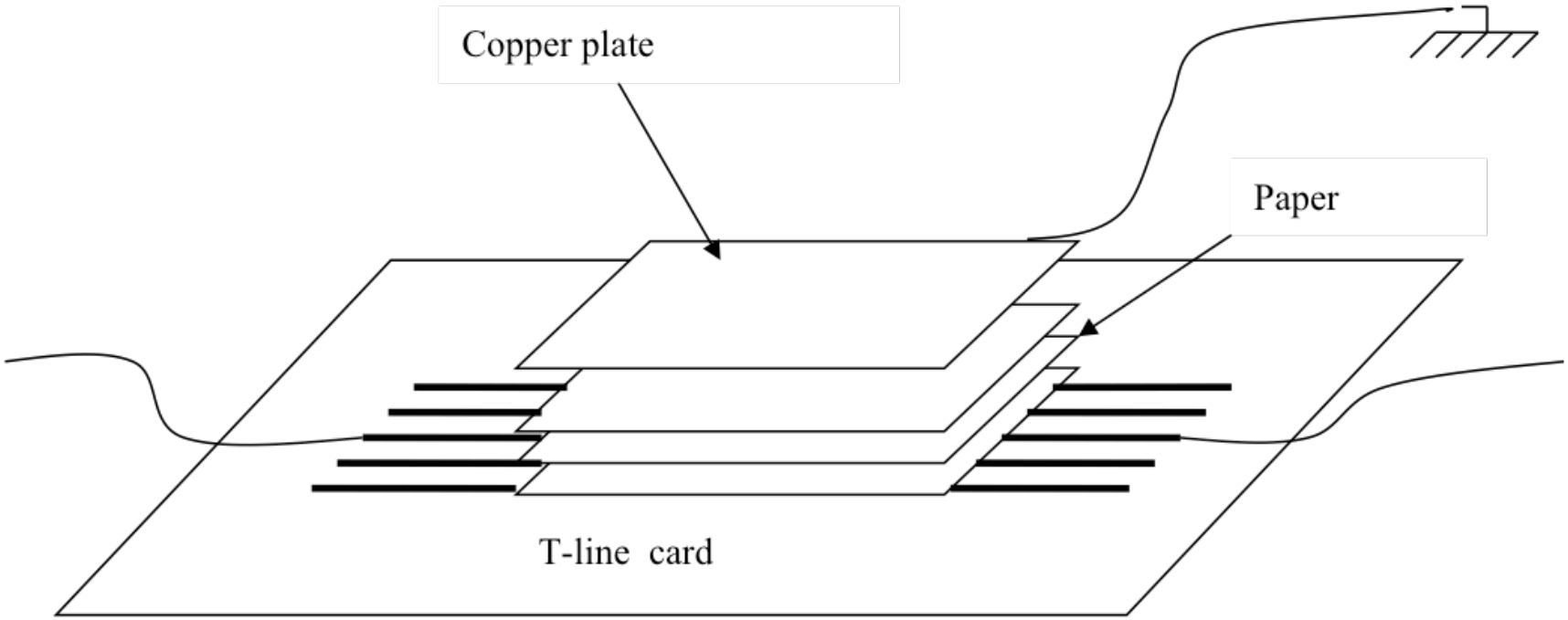
The Design



Simulated Impedance ≈ 50Ω

Simulated Analog Bandwidth = 1.5 – 2 GHz

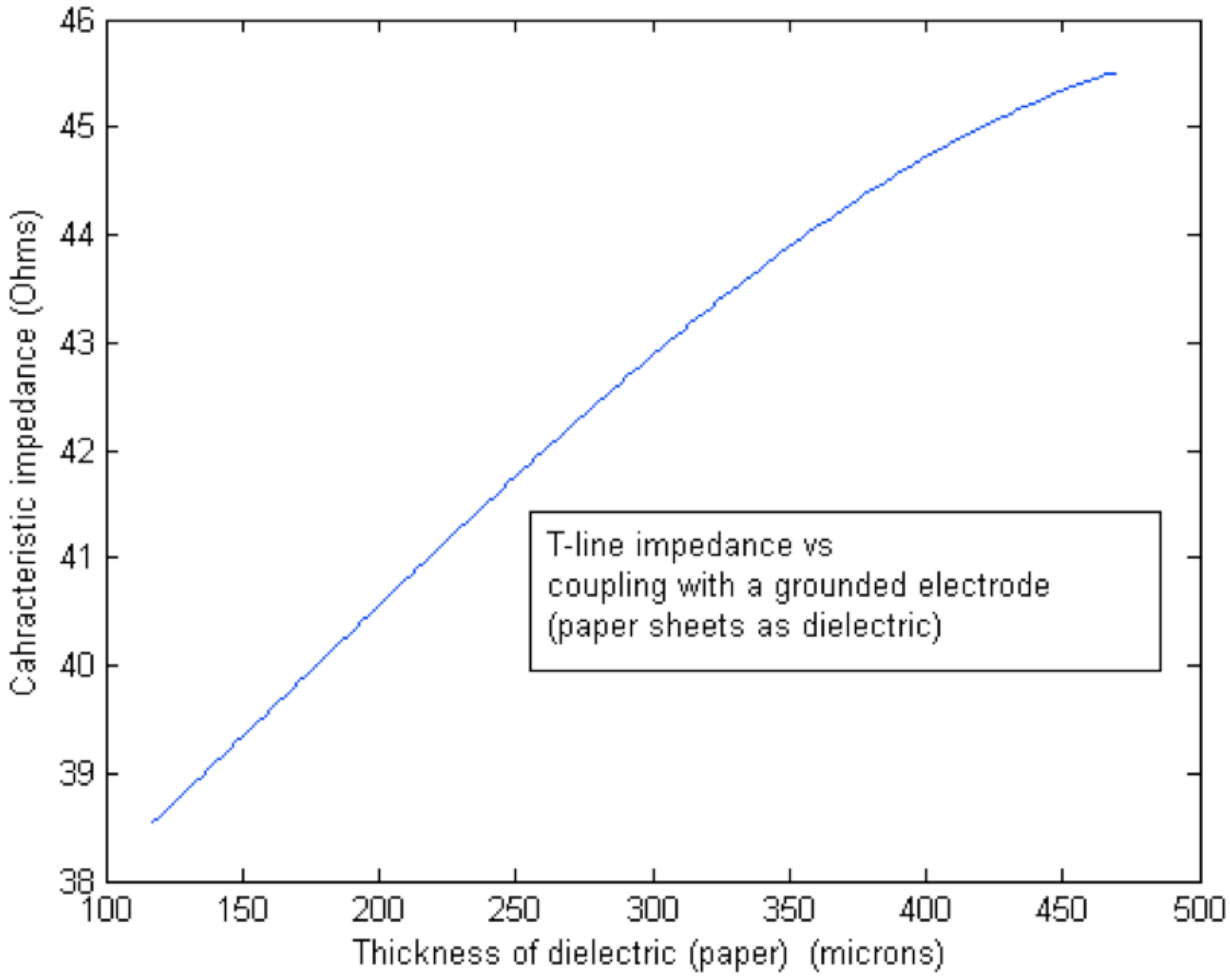
Jean-Francois' Experiment



Copper plate placed on top of stack of paper of varying height and measure any change in impedance with TDR (Time Domain Reflectometry).

Approximate the presence of the 2nd MCP since its bottom surface is conductive.

Results



Conclusion: 2nd MCP gap must be on the order of the anode thickness (≈500 µm) to minimize the effect of the MCP.

Impedance Matching

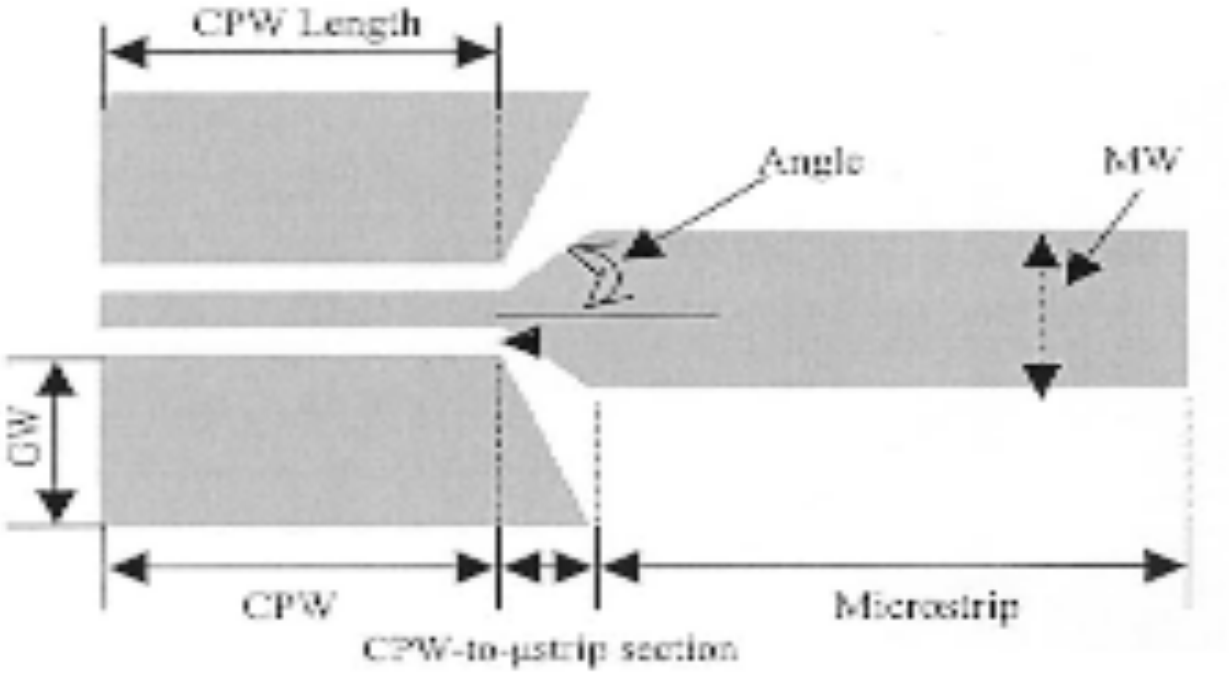
Option C

- Kovar Walls
- Large impedance discontinuity—strong coupling to kovar.
- Wall thickness of less than 2mm yield tolerable distortion.
- See PSEC Library

Option E

- Anode strips running under frit-sealed glass walls.
- Impedance decrease of only a few ohms—can be thicker than 2mm.

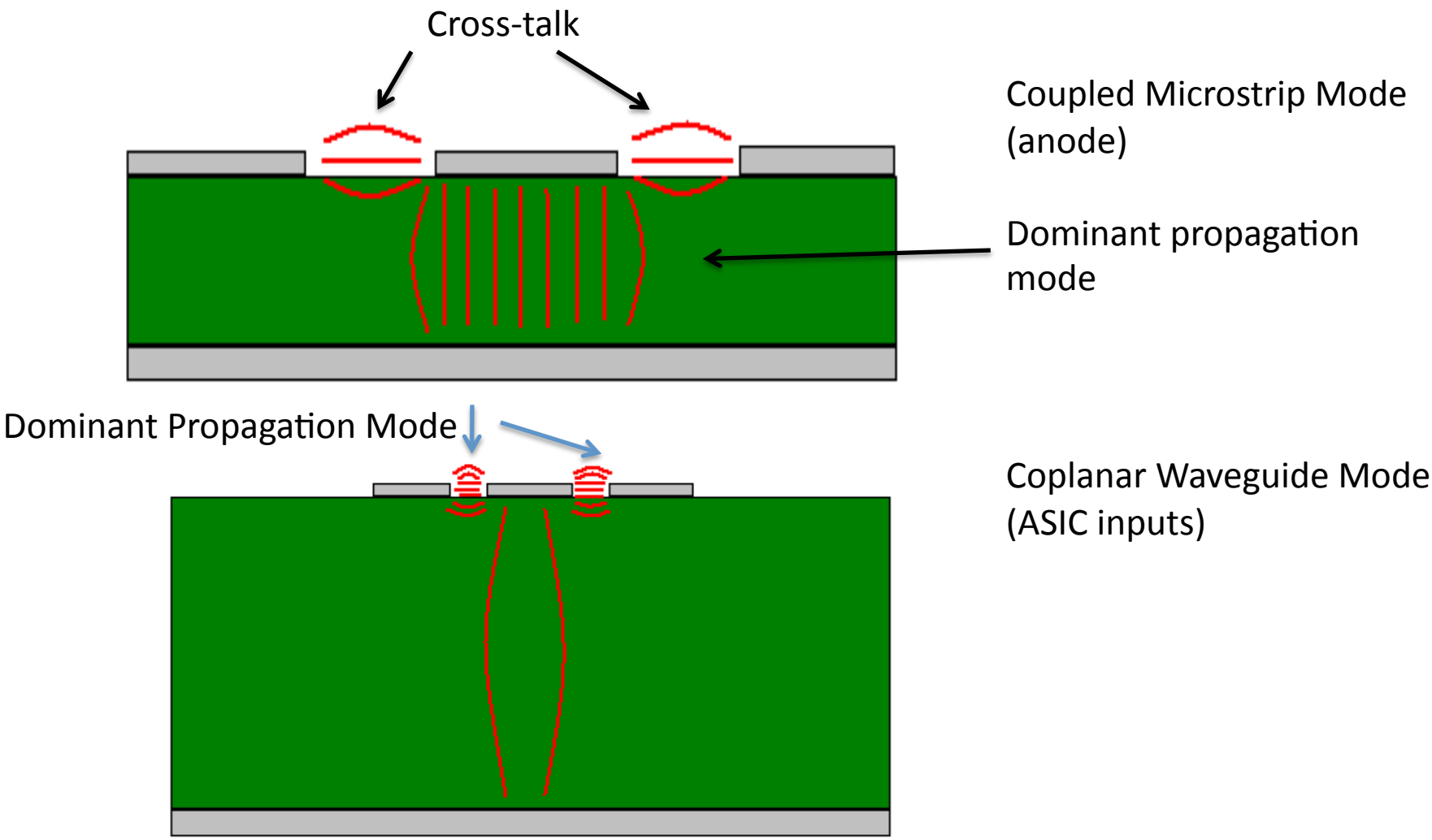
Microstrip to Coplanar Transition



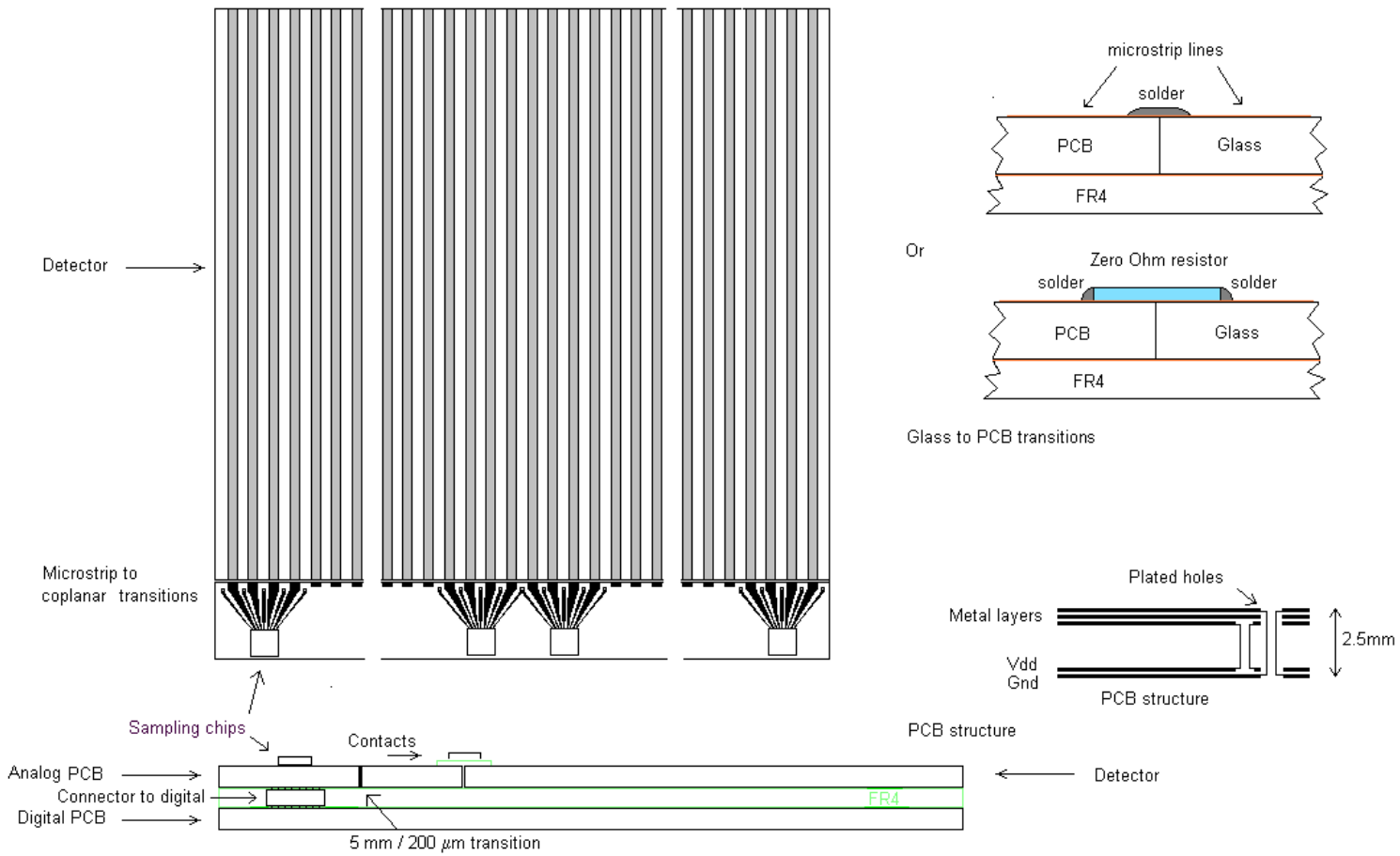
From Zheng, et al. "Wideband Coplanar Waveguide RF Probe Pad to Microstrip Transitions Without Via Holes." *IEEE Micro. and Wireless*. Vol. 13 No. 12. December 2003.

- Anode strips have signal layer on top and return path on lower ground plane; ASIC has signal and return path both on top layer.
- Need to design transition to preserve signal integrity and impedance matching as much as possible.

Field Matching



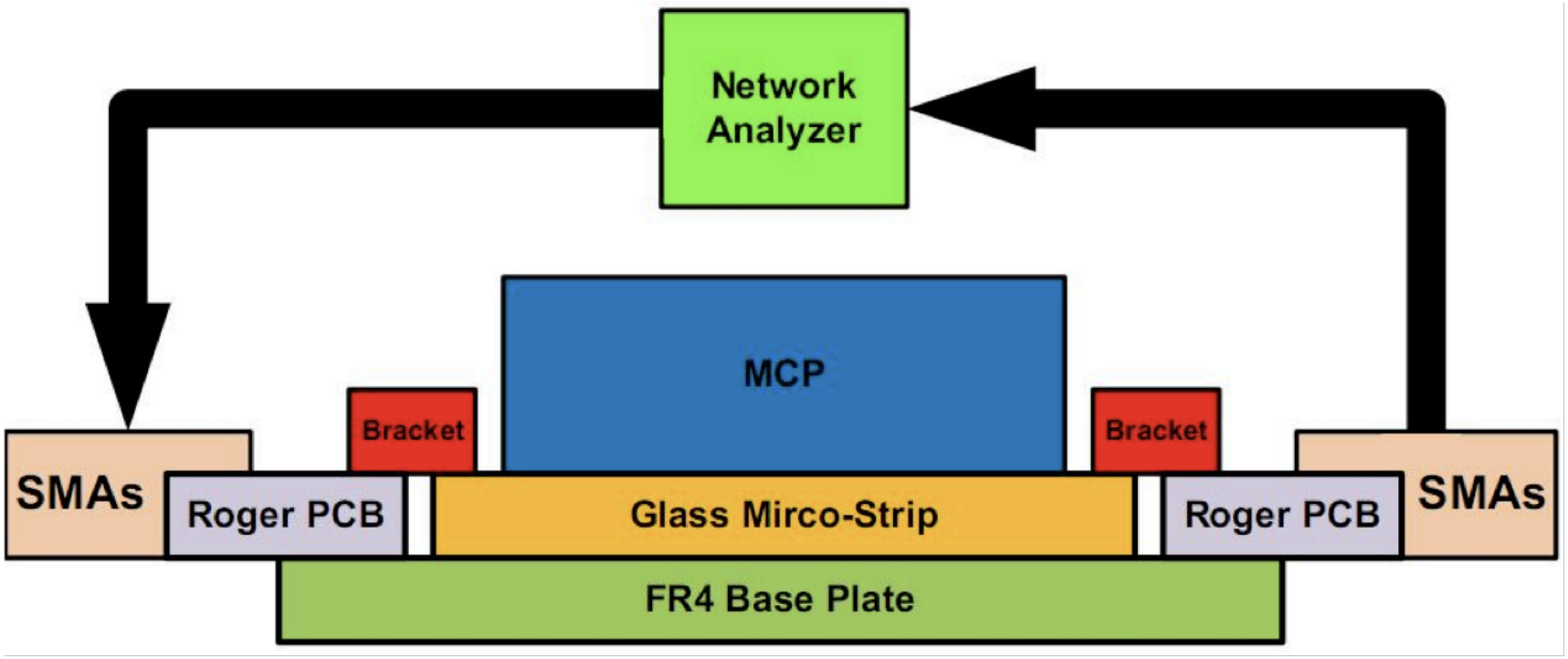
Proposed Anode-to-ASIC Coupling



Schedule

- Fabrication is beginning; we'll receive the first anode samples soon.
- Begin systematic electrical testing (bandwidth, impedance, dielectric properties, etc.)
- Begin design for complete test setup (anode-to-ASIC connection).

Anode Testing



Conclusion

- Signal Integrity is important in the design of the anodes and their connection to the ASIC.
- Perfection is not necessary, but bandwidth optimization and impedance matching are important especially at low SNR.
- Testing will begin as soon as fabrication is complete.

Extra Slides

Parameters

- 42 microstrip lines
- Top layer: 50nm Au
- Middle layer: at least 2 µm Ag.
- Bottom layer: 20-50nm Cr
- Also, Chromium pads to seal on sidewalls