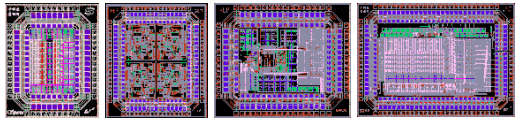
中国科学院高能物理研究所



# Collaboration between IHEP & CPPM on ATLAS Silicon Pixel Detector Upgrade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**Institute of High Energy Physics, CAS**

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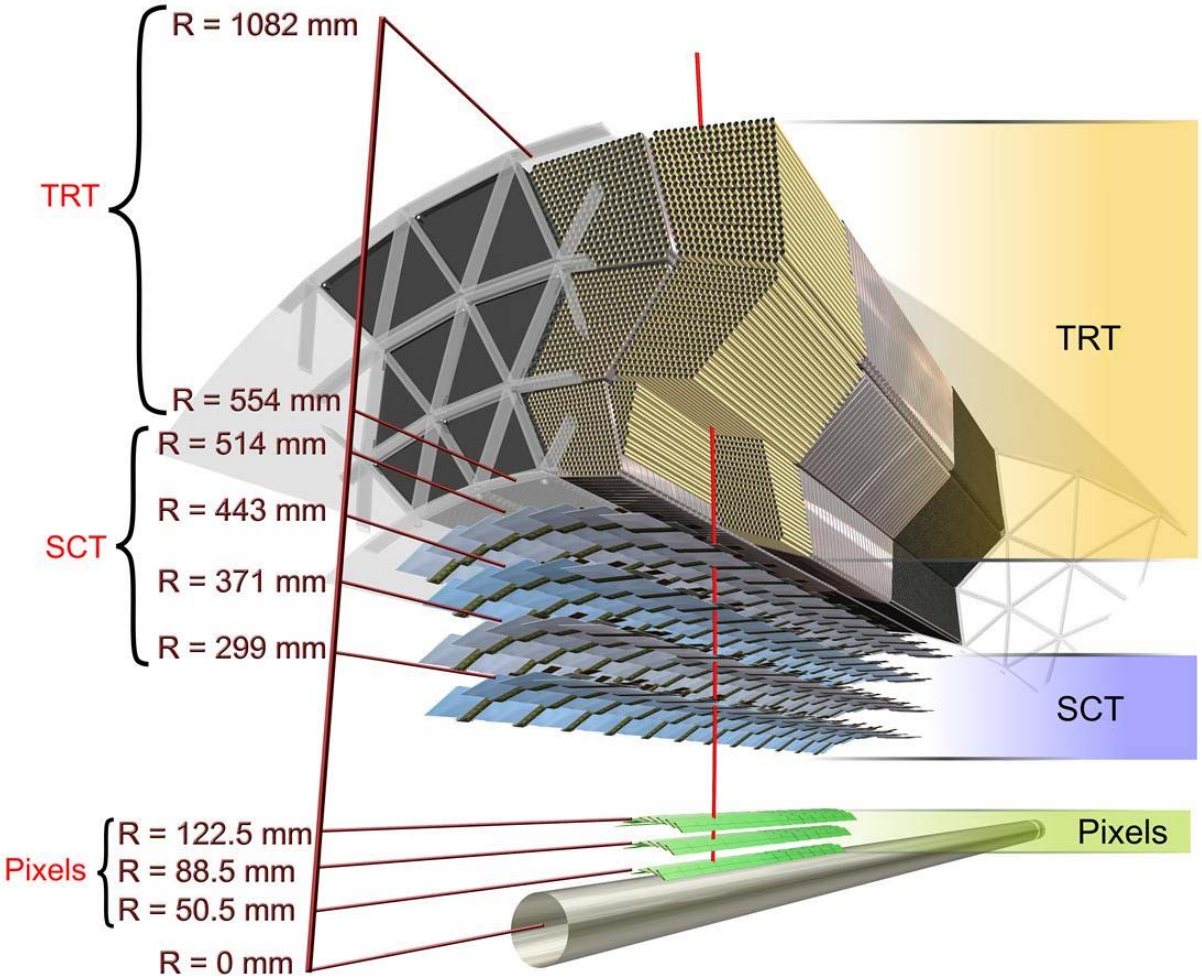
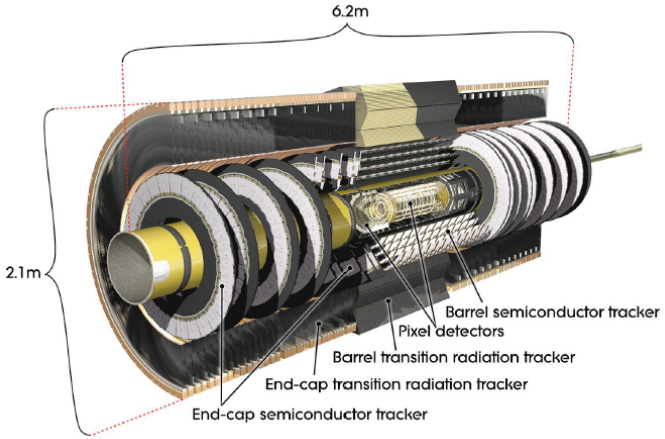
# Outline

- **ATLAS Silicon Pixel Detector Upgrade**
- **Collaboration between IHEP (Institute of High Energy Physics, CAS ) & CPPM (Centre de Physique des Particules de Marseille)**
  - **Building blocks design**
  - **Simulation, verification, & modelization**
  - **Measurement and firmware design**
- **Future Plan**

# Inner Tracking ATLAS detector




Straw tubes

Silicon strip

Silicon pixel

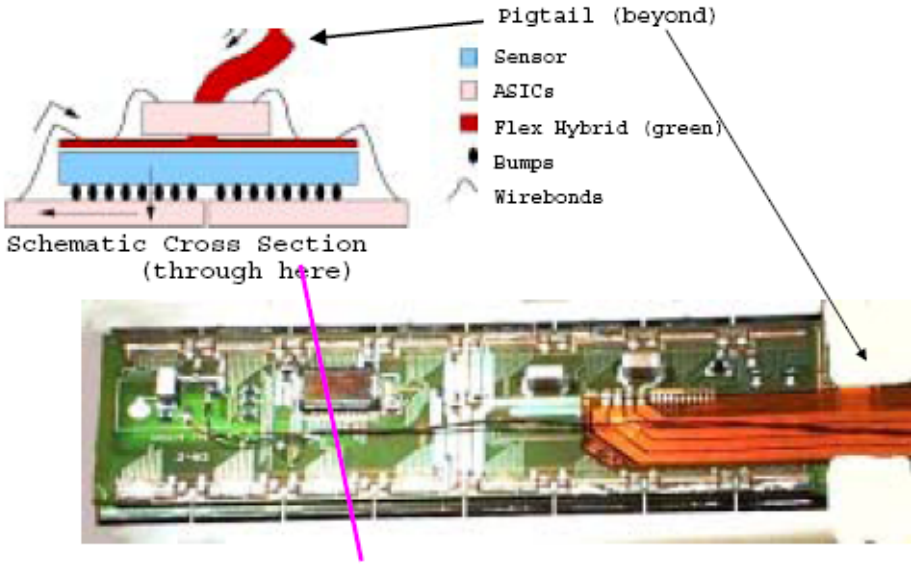
# ATLAS Silicon Pixels detector

**Read-Out electronic:**

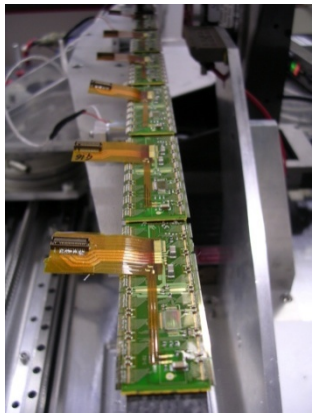
50µm * 400 µm pixel size

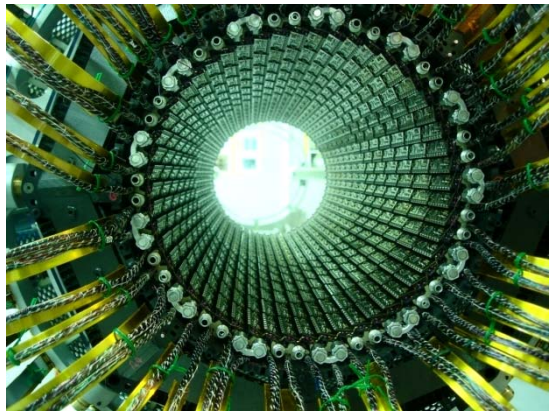
FEI-3 circuit : IBM 0.25 µm technology

**Collaboration institutes**
Bonn University, Germany ; LBNL, USA ; CPPM, France (in the initial stages)

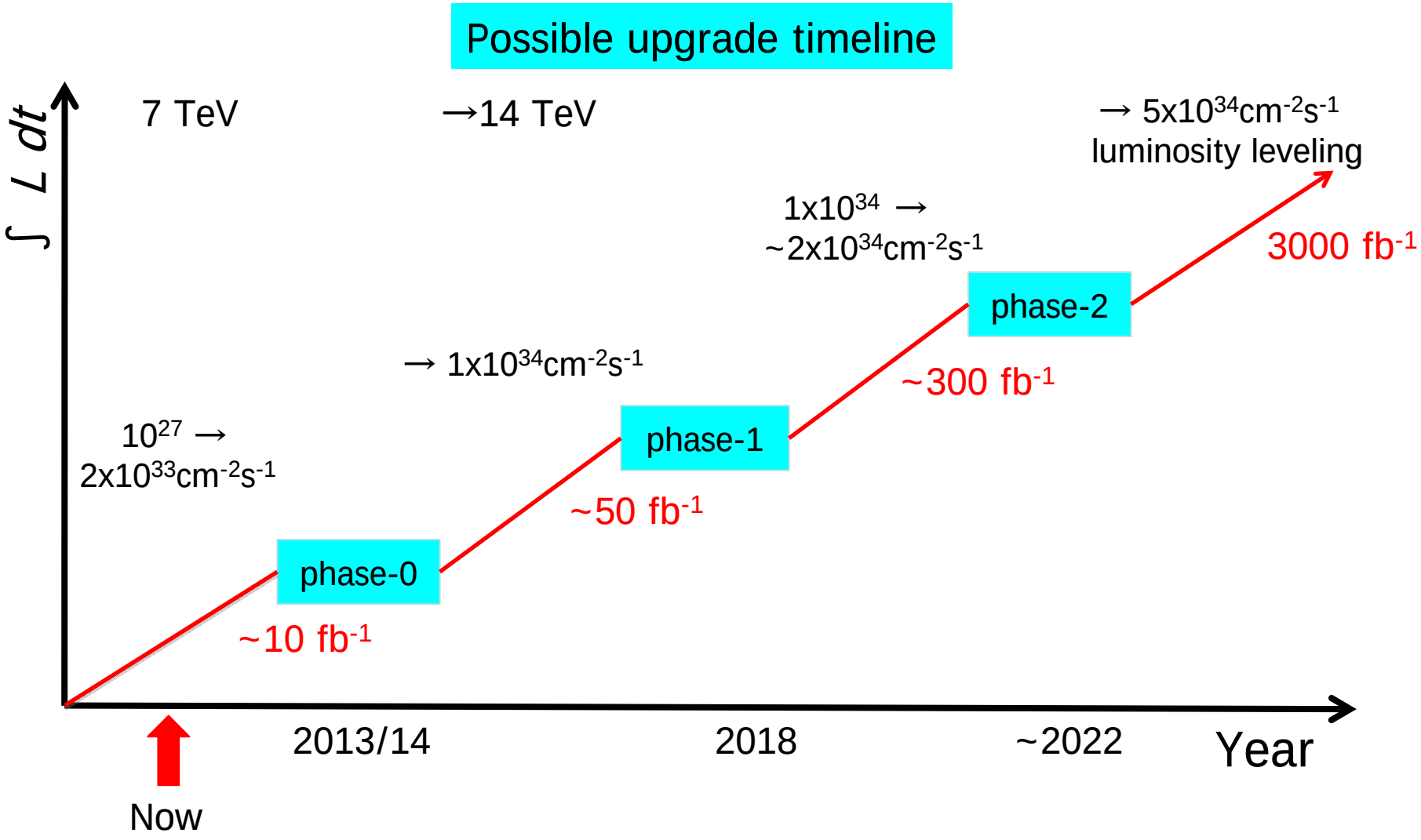



Like a big camera with a 1.7 $m^2$ area and 86 Million of Pixels with a snapshot every 25ns





# LHC and ATLAS upgrade




ATLAS needs to maintain excellent position resolution (vertexing, tracking)

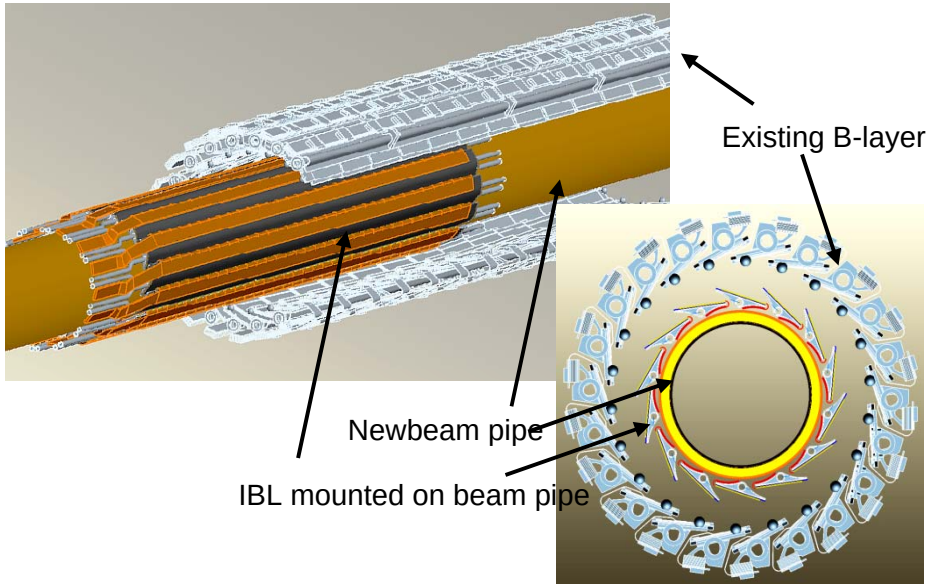
# ATLAS upgrade : phase - 0

- The current B-layer will become inefficient
- after phase-1 (beyond nominal luminosity):

- data bandwidth, radiation damages, …

- The idea is, instead of replacing the B-layer,
- which is very difficult and dangerous,
- add a new B-layer inside the present one.

- 3 pixel layers → 4 pixel layers




- Insert the new layer inside the current beam pipe (Insertable B-Layer → IBL)
- using a smaller beam pipe.

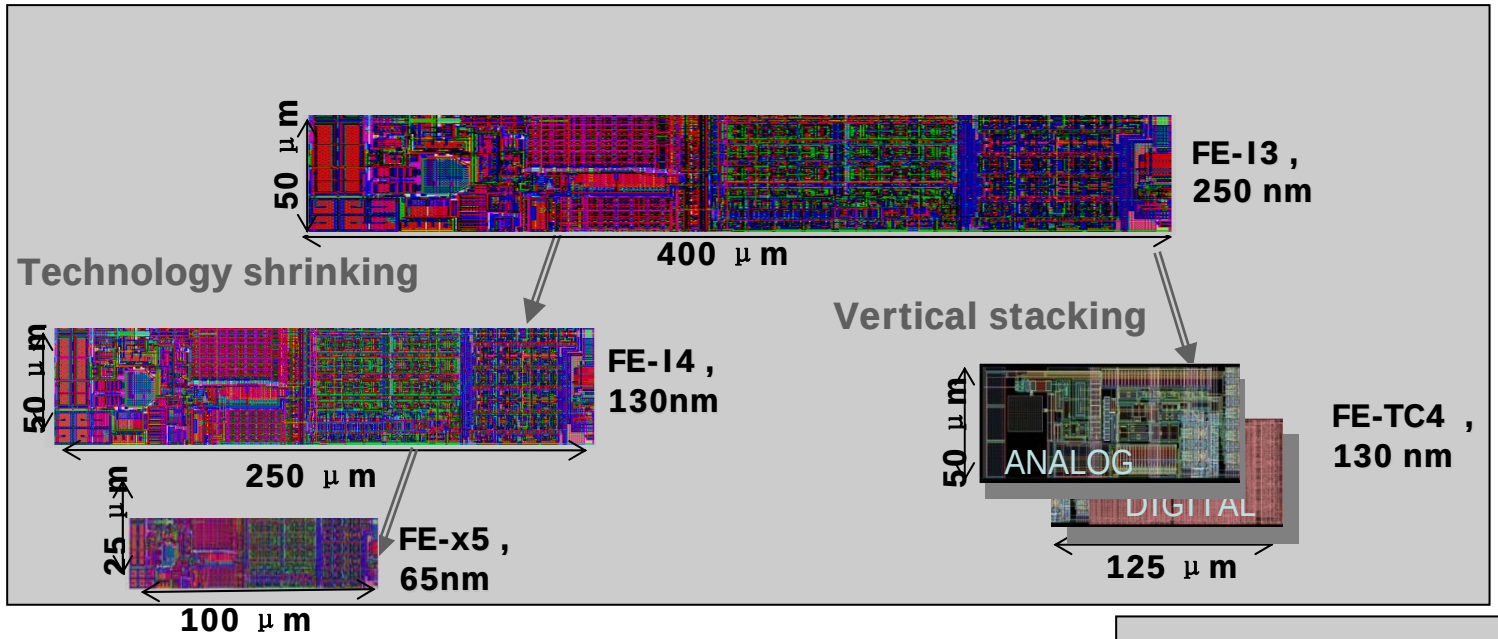
- Phase-1 was initially in 2016, now it is postponed to 2017 or 2018,
- → Advance the project schedule and install in 2013/2014.

- it helps anyway, improves performance
- less activation in earlier time (ease of installation)

# Motivations for ATLAS read-out chip upgrades – Phases 1 and 2

- Improve spatial resolution
- Deal with an increasing counting rate

} • **Decrease pixel size**




First MPW run for High Energy Physics organized by FNAL with a consortium of 15 institutes.

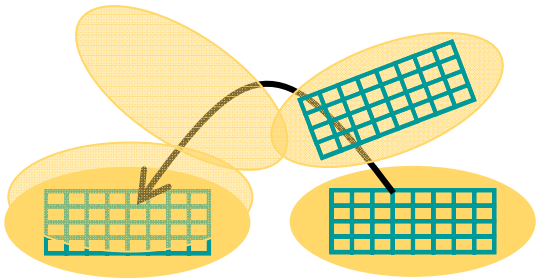
The proposed 3-D process combines :
**GLOBAL FOUNDRY 130nm technology**
**TEZZARON 3D technology**

3-D benefits :
Pixel size reduction
Functionalities splitting
Technologies mixing

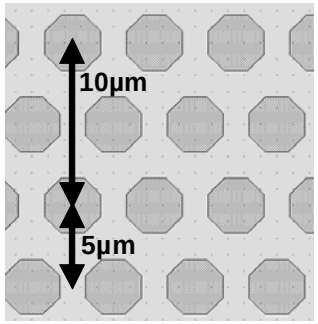
# Tezzaron-Chartered 3-D technology

**Main characteristics :**

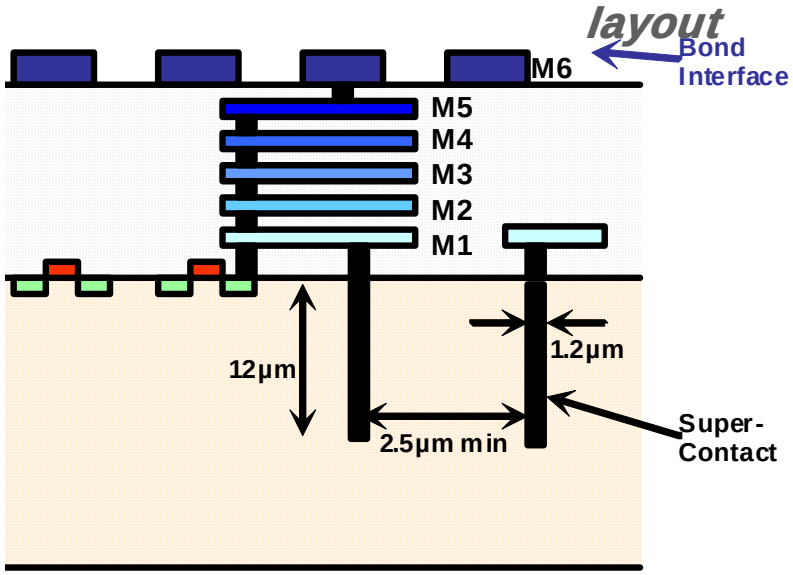
- **2 wafers** (tier 1 and tier 2) are stacked **face to face** with Cu-Cu thermo-compression bonding
- **Via Middle** technology : **Super-Contacts** (Through Silicon contacts) are formed before the BEOL of Chartered technology.
- Wafer is **thinned** to access Super-Contacts
- Chartered 130nm technology limited to **5 metal levels**
- **Back-side metal** for bonding (after thinning)



*Wafer to wafer bonding*




*Bond interface layout*

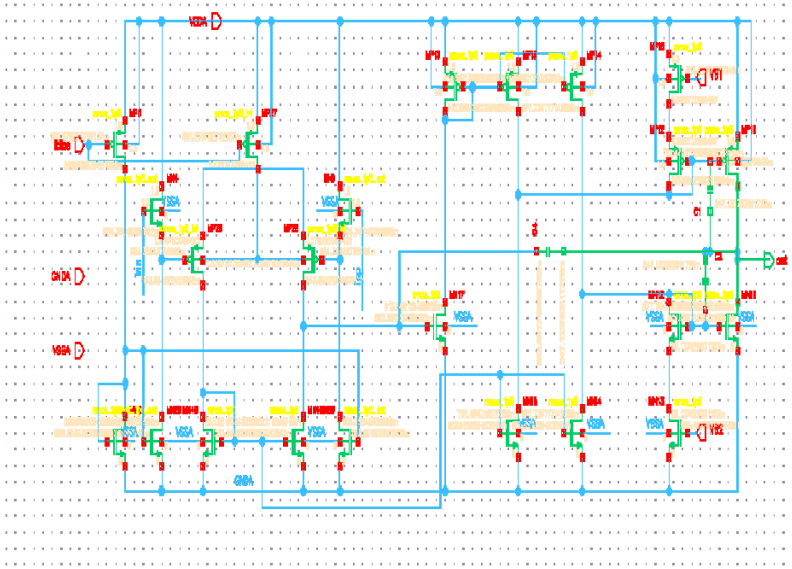


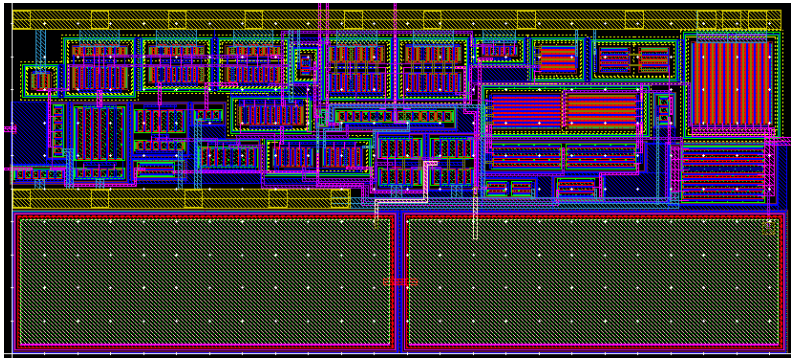

*One tier*

## Collaboration between IHEP & CPPM on ATLAS Pixel Detector

- **Since 2009**
- **IHEP is aiming to fully participate in the collaboration of ATLAS Silicon Pixel Detector Upgrade, especially on 3D approach**
- **Collaboration with CPPM on Pixel Detector ASIC design**
  - **Phase 0 & Phase 1**
    - **Irradiation test firmware setup**
    - **Building Blocks design**
    - **Simulation and debug**
    - **Layout and tapeout preparation**
    - **Chip Measurement**
  - **Phase 2 & future**
    - **Initial design on 65nm process**

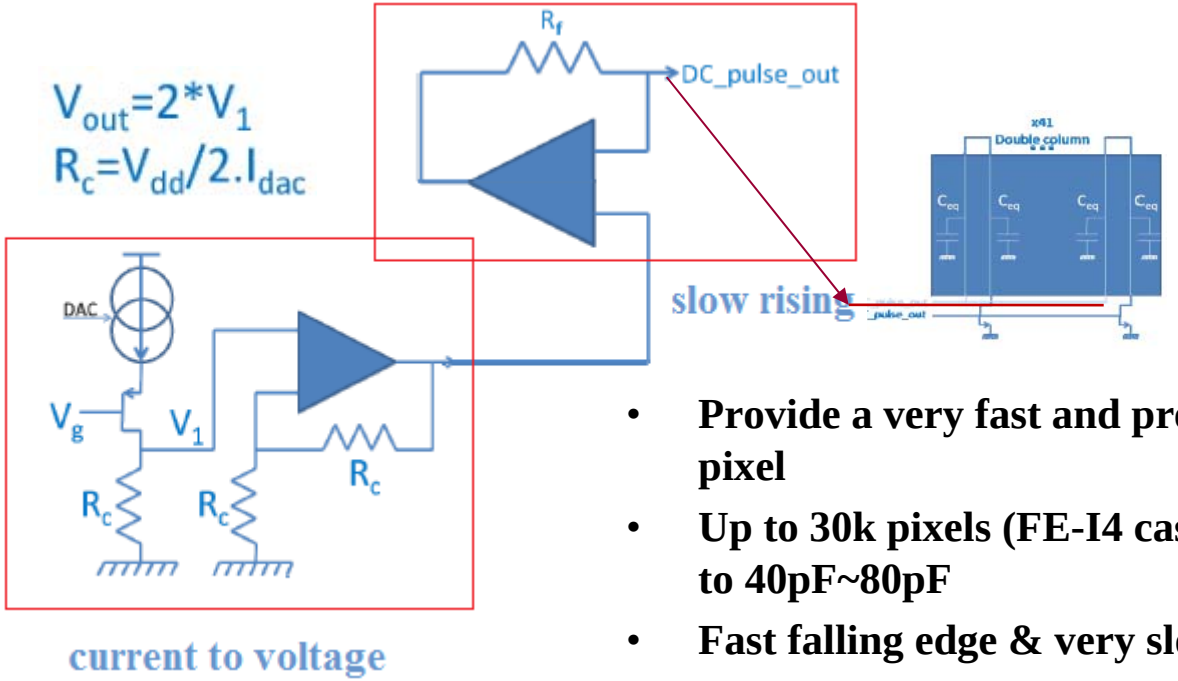
# Building blocks design – Monitoring Buffer



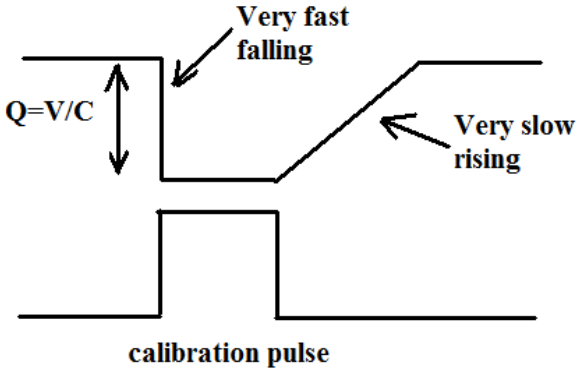


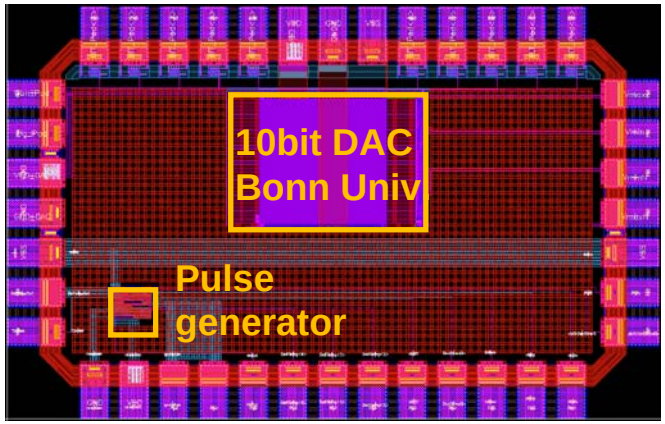
- **One of the new building blocks in FE_C4_P2 chip**
- **To probe and buffer out all the critical nodes in pixels**
- **Full-scale in/out range**
- **Specification:**
  - **$C_{load\ max}$=50pF $R_{load\ max}$=1Kohm**
  - **Bandwith @unity gain: 60MHz**
  - **Slew rate : 29V/ μ s**
  - **Power on quiescent current : 1.6mA(Vinputdc=100mV)~3.5 mA(Vinputdc=1.4V)**
  - **DC gain : 49dB**
- **Designed in March, 2010 by J. Luo**
- **Working well by measurement, reused in the following pixel chips**

# Building blocks design – Calibration block



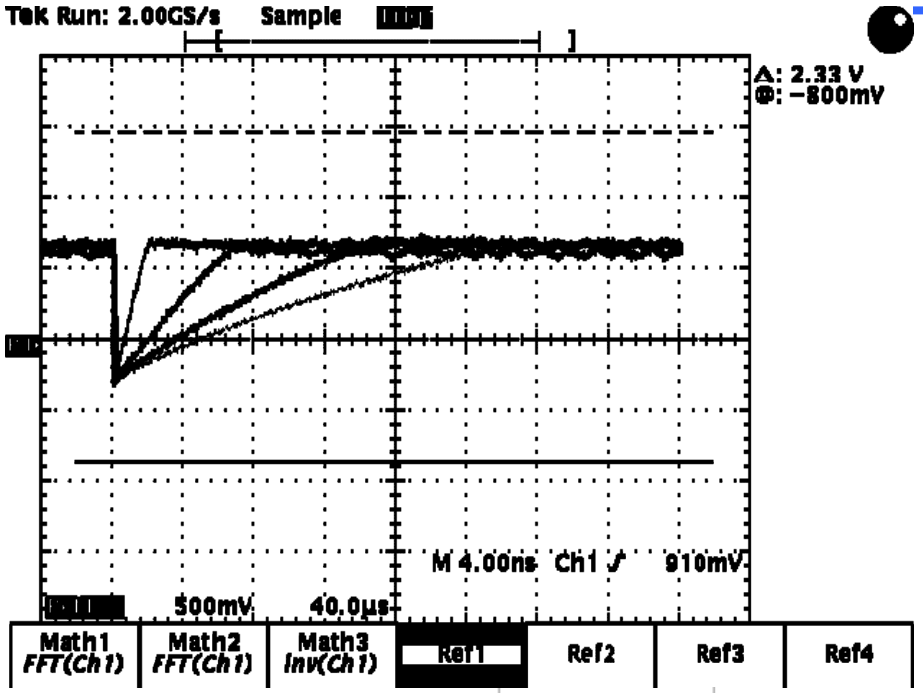

current to voltage



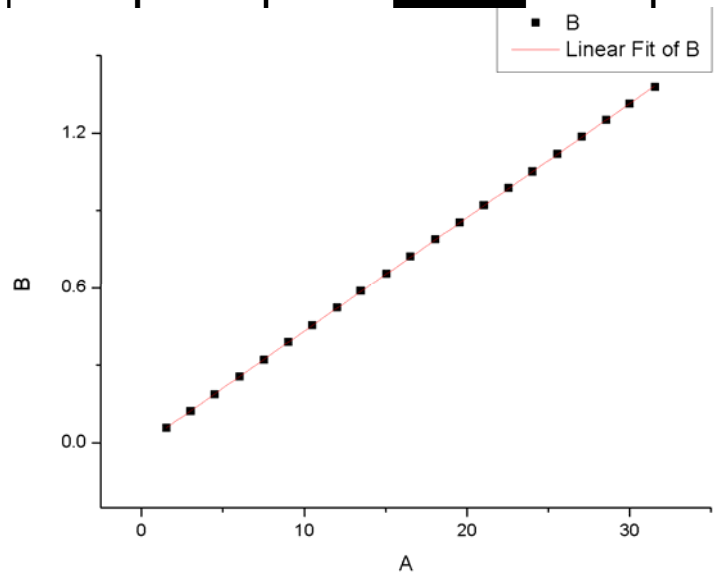



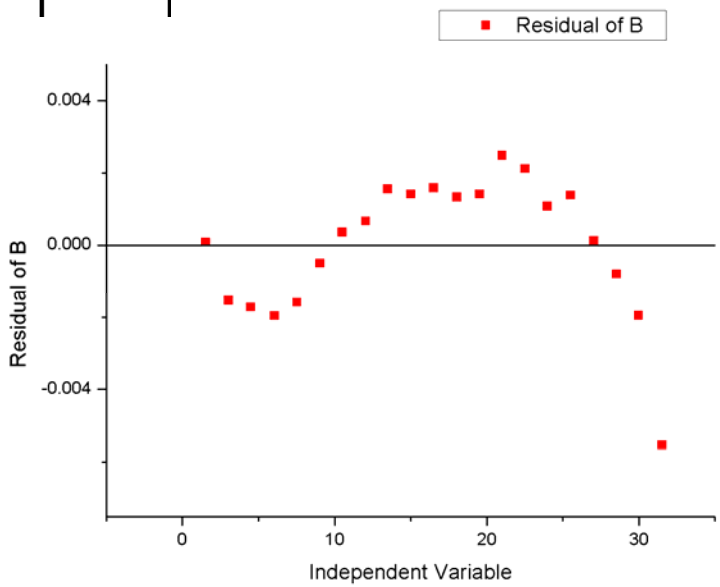

- **Provide a very fast and precise calibration pulse to every pixel**
- **Up to 30k pixels (FE-I4 case), parasitic capacitive load up to 40pF~80pF**
- **Fast falling edge & very slow rising edge**
- **Capable of pulse phase tuning and rising time tuning**
- **Building blocks chip FEC4_P3C (with Bonn Univ.)**
- **Submission: Nov. 10, test: March 11, by W.WEI**
- **Specification:**
  - **Dynamic range: 0 ~ 1.5V**
  - **Load capacitance: 40pF ~ 80pF**
  - **Falling time: < 2.5ns@ far end pixel**
  - **Rising time: 20 μ s~500 μ s, 3bits tunable**
  - **calibration linearity: 0.5%**

# Measurement for single block




- **Falling time for charge injection: < 4ns @ 2ns stimuli pulse**
- **Rising time tuning:**
  - **Overlapped snapshots from four measured outputs with different tuning bits configuration( 001/011/101/111)**
  - **Showing rising time is tunable 20~400 µs**
- **Dynamic range: Better than 1.4V**
- **Linearity: <±0.5%**
- **Similar results as in simulation**



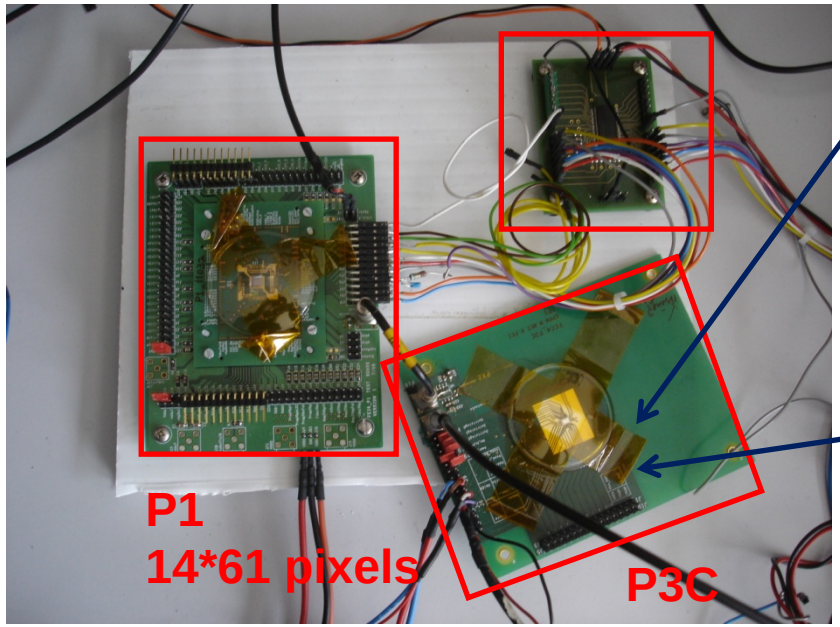
# FEC4_P3C & FEC4_P1 combined system

Volt controlled by GPIB

Keithley 2410
V/I SourceMeter

CPPM current source module

USB Interface

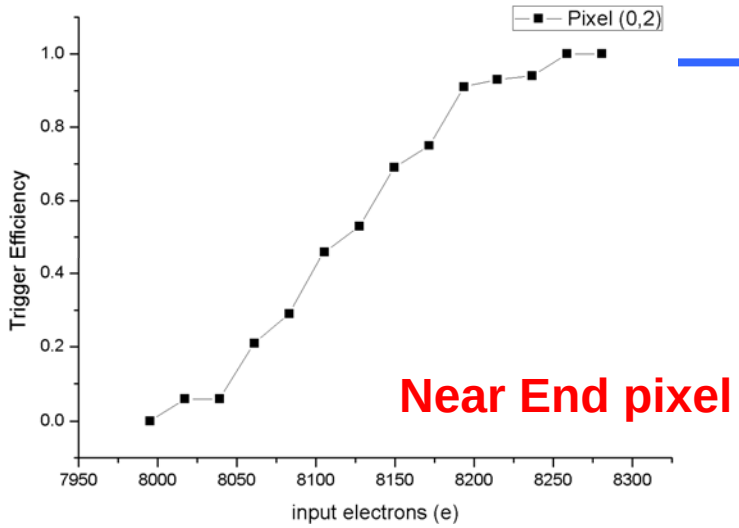



Current Output
Controlled by Keithley

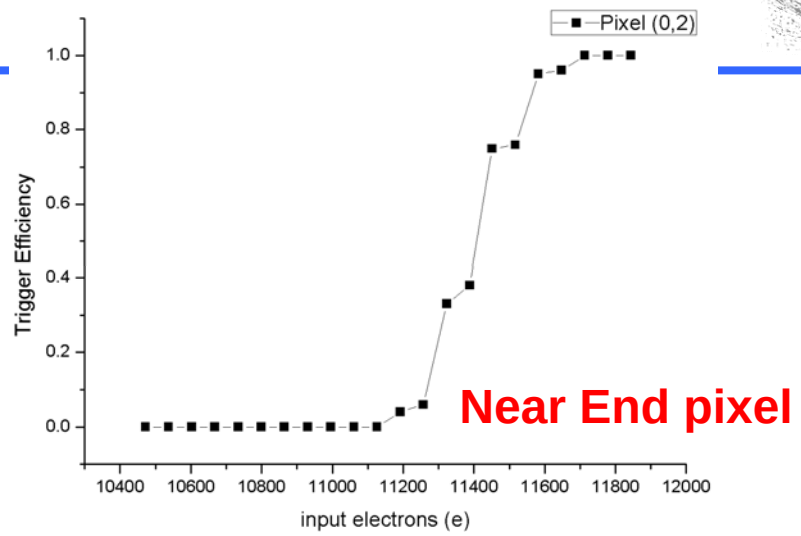
Calibration pulses output

HP8110A Pattern generator

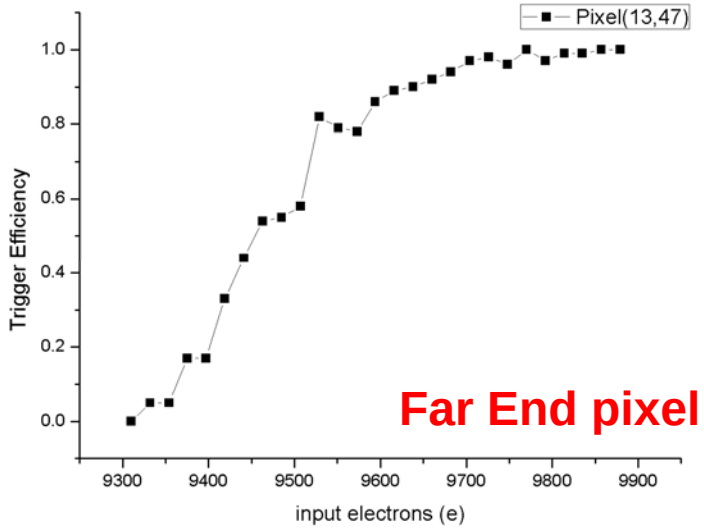
# S-curve measurement



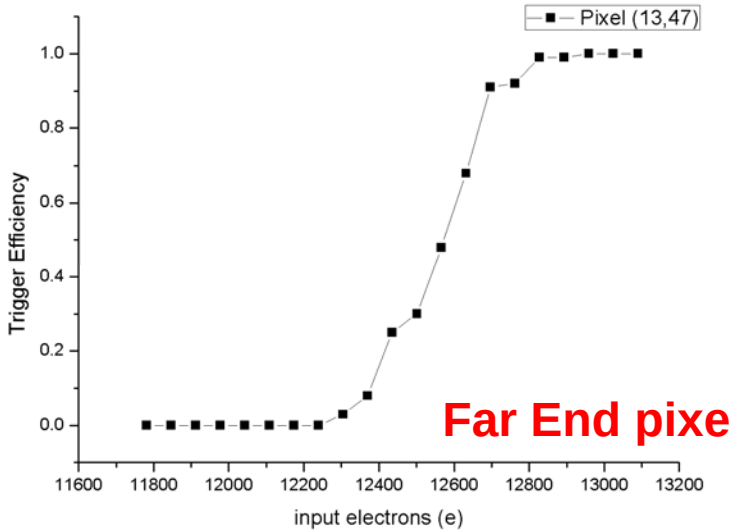

**Pixel (0,2) HP generator + P1**
**Rms = 50e, 50% threshold =8117e**




**Pixel (0,2) P3C generator + P1**
**Rms = 104e. 50% threshold =11409e**

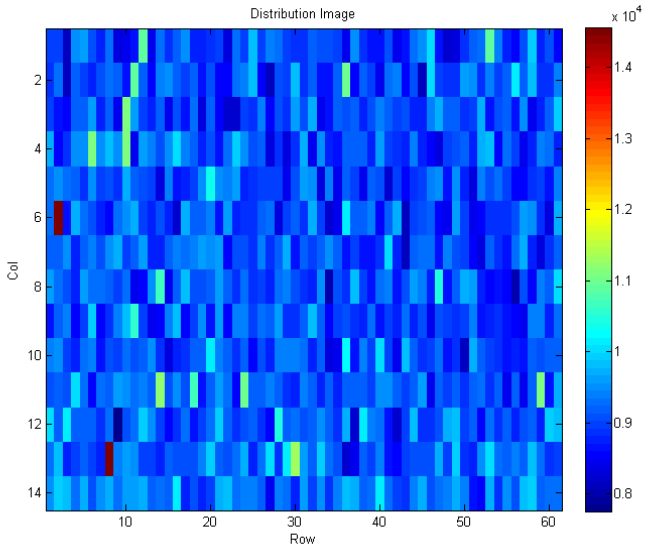



**Pixel (13,47) HP generator + P1**
**Rms = 95e, 50% threshold =9454e**

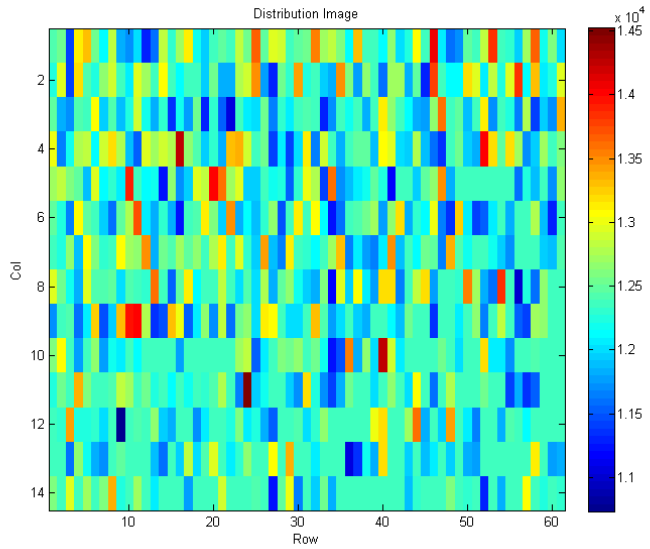



**Pixel (13,47) P3C generator + P1**
**Rms = 109e, 50% threshold =12572e**

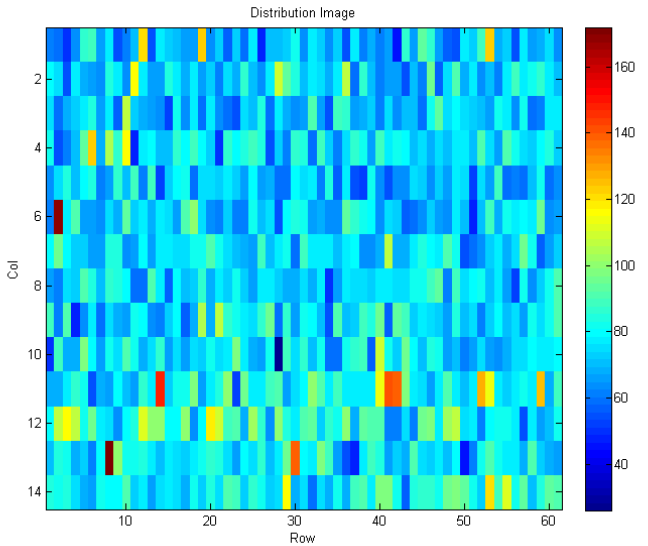
# Full chip scan image



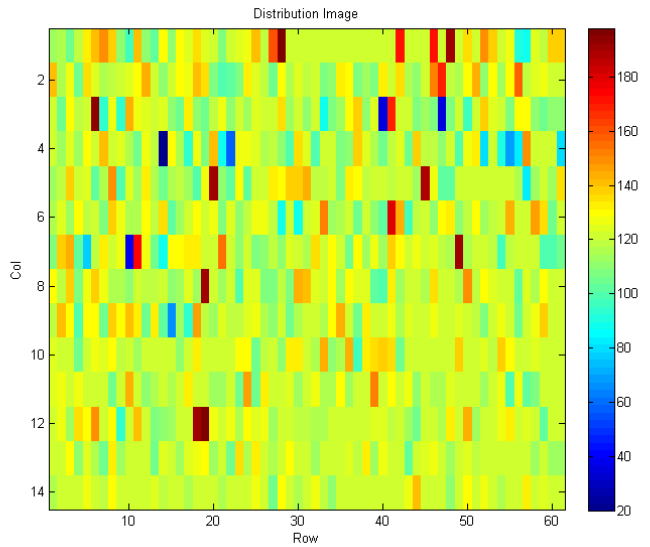

HP generator + P1, threshold distribution




P3C generator + P1, threshold distribution

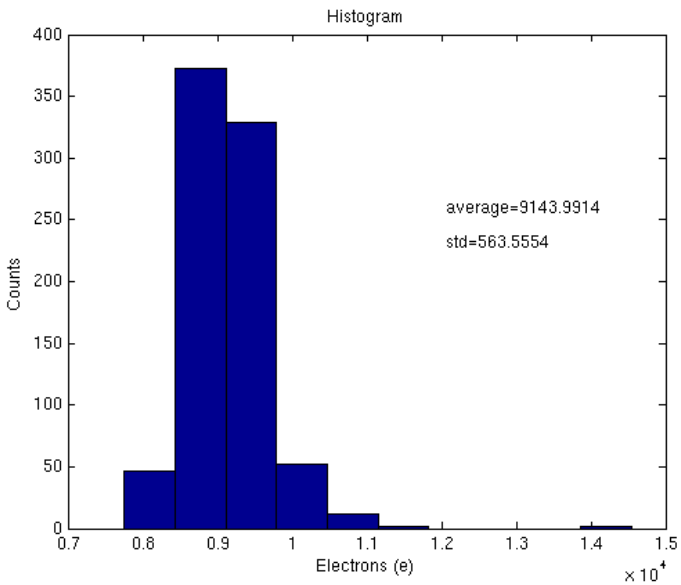



HP generator + P1, noise distribution



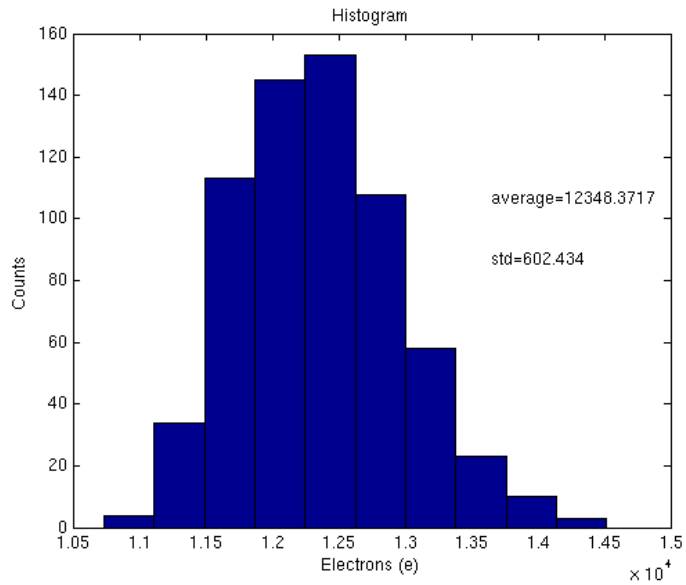

P3C generator + P1, noise distribution

# Dispersion comparison



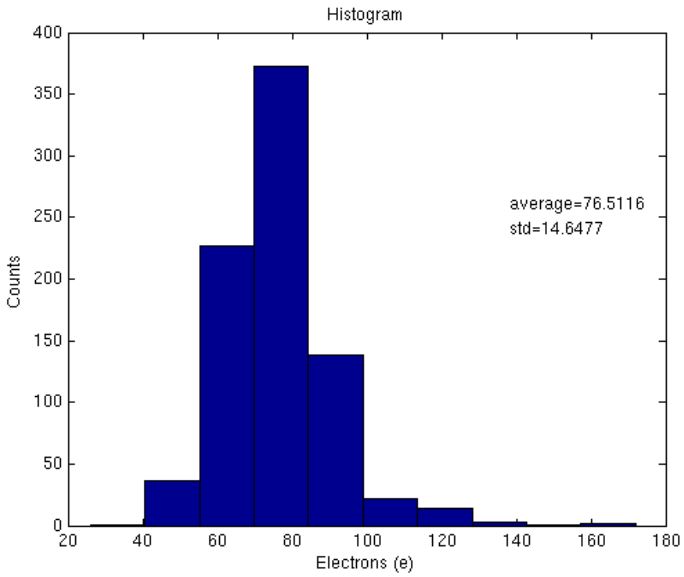

**Aver=9.1ke**
**std = 563e**

**HP generator + P1, threshold histogram**



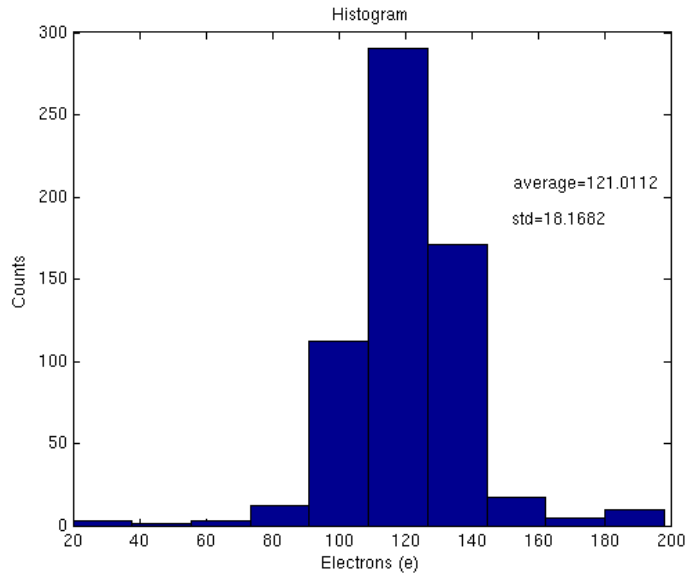

**Aver=12ke**
**std = 602e**

**P3C generator + P1, threshold histogram**




**Aver=76e**
**std = 14.6e**

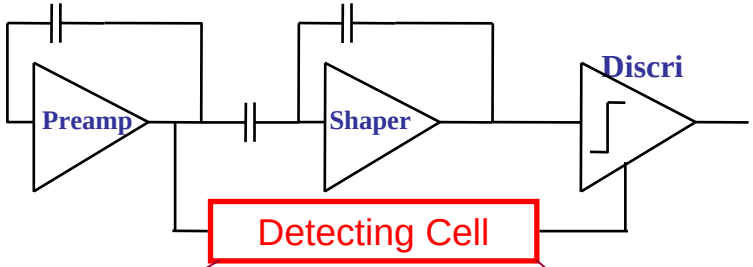
**HP generator + P1, noise histogram**

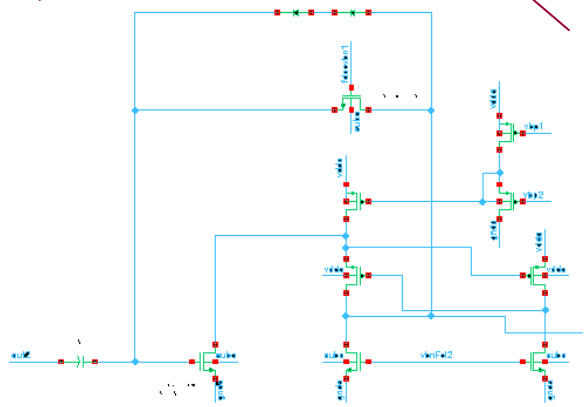



**Aver=121e**
**std = 18.2e**

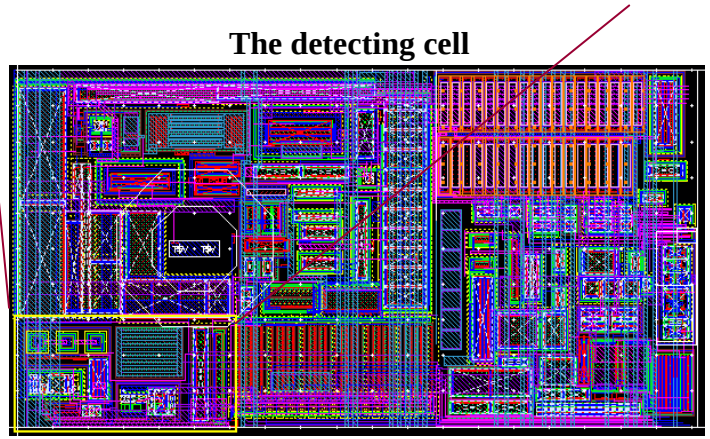
**P3C generator + P1, noise histogram**

# Building blocks design – A new low power pixel cell



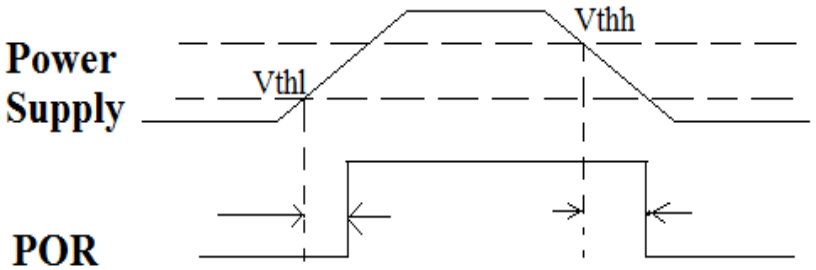
The detecting cell

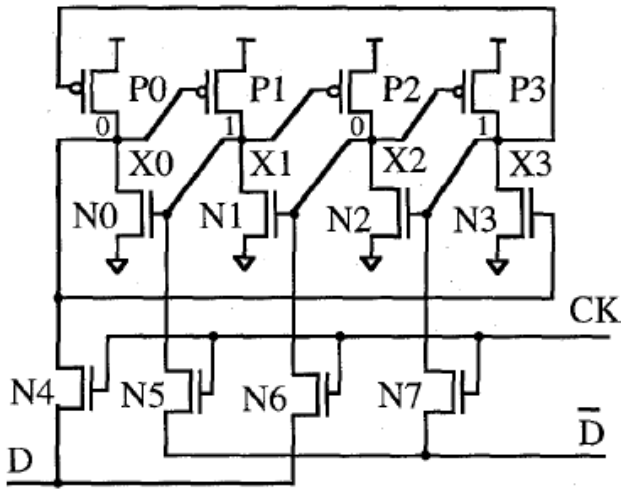


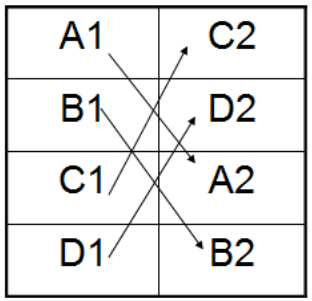
New pixel design with power-down

- **To save power:**
  - **Design optimization (static)**
  - **Sleep – low power standby – wakeup – working – sleep (dynamic)**
- **A most power consuming block: discriminator (4 μA → 1.2 μA)**
- **Design issue:**
  - **Very large gain: Preamp output → Digital level**
  - **Speed: Wakeup pulse to be faster than TOT output**
  - **Area: very limited space in the exsited pixel design**
  - **Low power: ultra low self power consumption**
  - **Input charge range: 1k $e^-$ ~ 100k $e^-$ (full)**
- **Special design:**
  - **DC close loop, AC open loop for large gain**
  - **Clamp for large signal stabilization**
- **Designed in Dec. 2011, by W.WEI**
- **Will be included for two columns in the next 3D run**

# Other building blocks design




4-latch cell

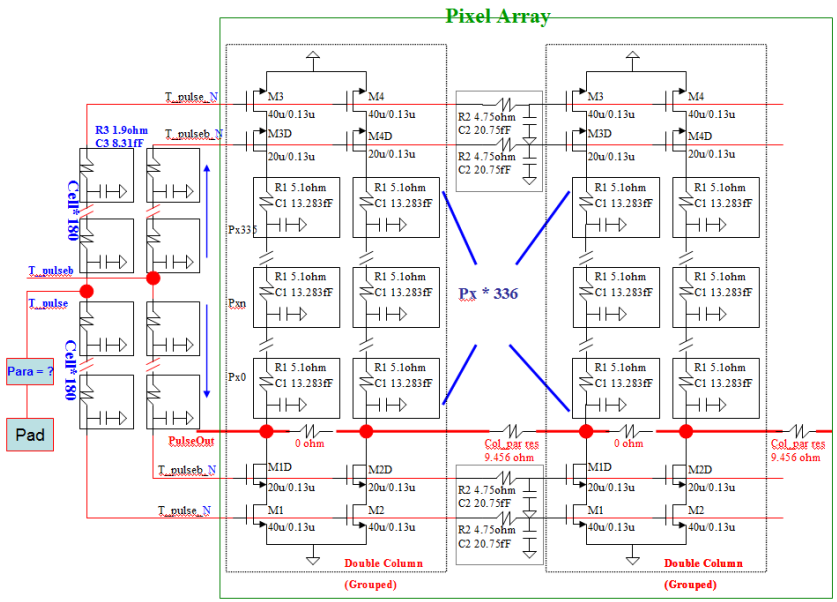
- **Power-on-reset block**
  - **Reset signals generated on both of the rising and falling edge of power supply**
  - **Compatiable with both 1.5V and 1.2V supply**
  - **Hysteresis of 100mV**

- **New layout of the DICE latch**
  - **Based on the 4-latch cell**
  - **Further separate the complementary node, enhance the anti-SEU capability**
  - **Layout size shrunk**

# Chip Design – full chip functional simulation

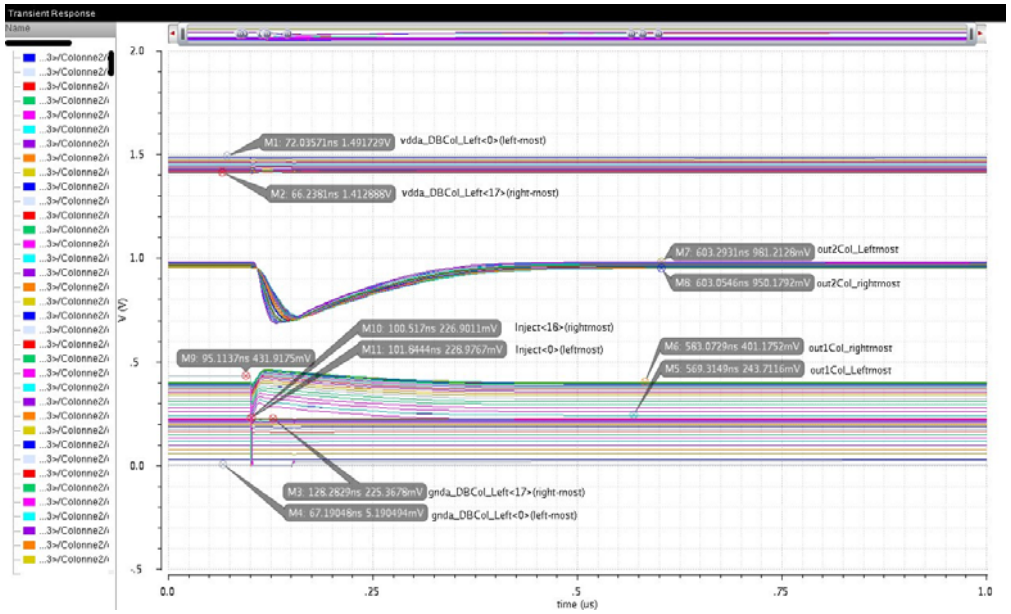
- **Full chip overall simulation**
  - **Common simulation: configuration of pixels are preset, configuration phase ignored**
  - **Real case of operation: configuration → normal operation time consuming in simulation**
  - **Overall simulation by FastSpice (Ultrasim):**
    - **Work as in the real case**
    - **Evaluate all the bias settling**
    - **Evaluate the configuration process and compatiability with PUC**
  - **Debug: Problems of HitEn, ClrGlobal, LdEn… in FEC4_P3 were solved**
- **Full chip power network layout evaluation**
  - **Power distributed as a non-ideal grid with para. R**
  - **IR Drop: Bias condition may vary from near end to far end**
  - **FastSpice (Ultrasim Power Network Solver) with estimated R from layout extraction, to evaluate IR Drop and bias of all pixels**

# Full chip power/bias network modelization




- Probe critical node performance
- Verify if the variation caused by power/bias distribution is acceptable

- Parasitic extraction
- Modelization according to the pixel matrix parameter
- A 60row×336col pixel matrix modelization

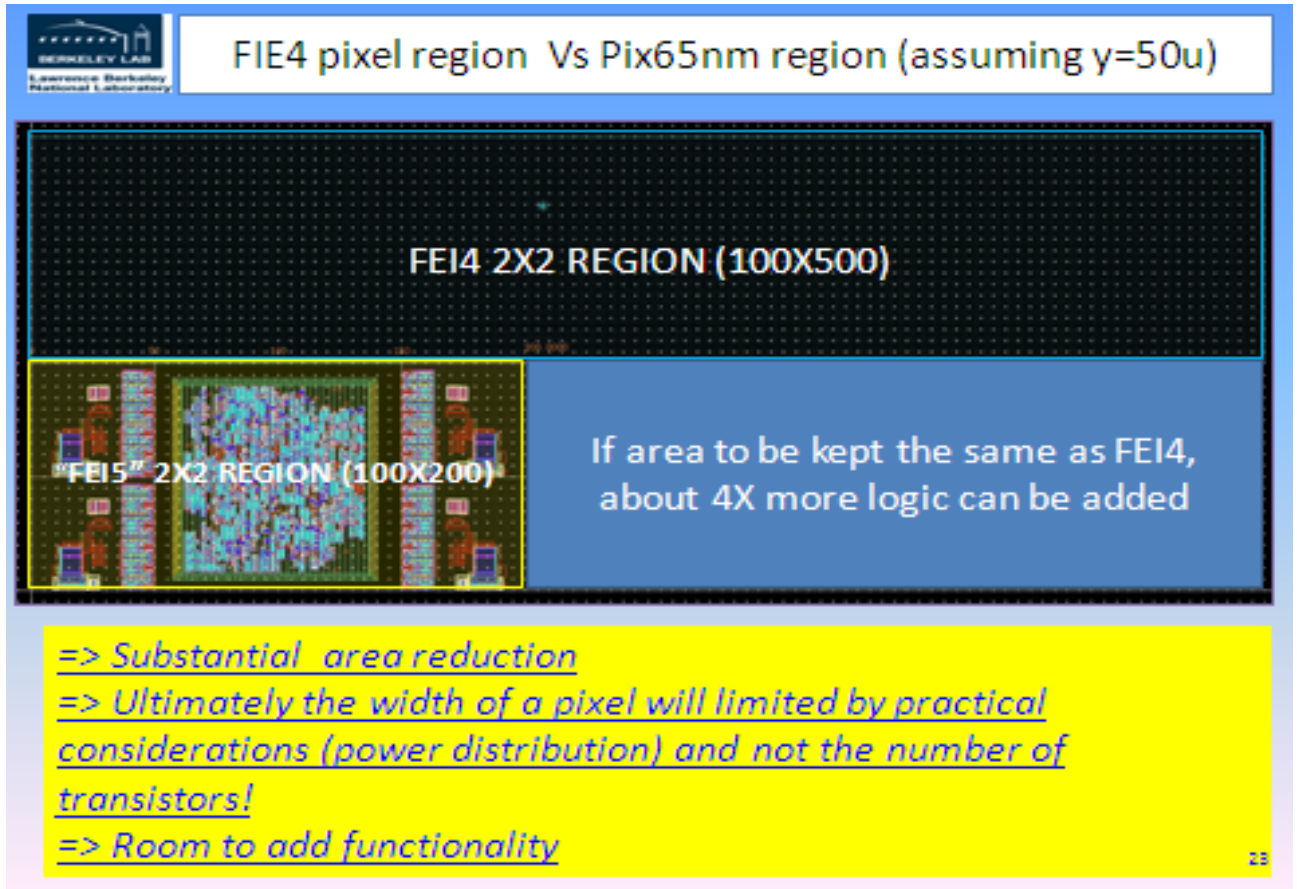


# Layout & tapeout preparation for the next 3D run

- **The next 3D run in Tezz-Char expected at the end of 2012**
- **Layout and tapeout preparation:**
  - **Process transform:**
    - **From standard Chartered 130nm to Tezz-Char 3D process**
  - **Pixel matrix: re-organized and re-layout of three options:**
    - **Classical pixel**
    - **Modified pixel design with power-down**
    - **Modified pixel design with bias and latch optimization**
  - **Global Configuration Memory:**
    - **Adding triple redundancy bits read-back chain for SEU monitoring**
  - **New building blocks integration:**
    - **Calibration, power-on-reset, ref-current generator …**
  - **Full chip simulation with parasitic**

# For future design

- **Collaboration on future 65nm process also started, with both CPPM & LBNL**
- **More space, more challange**



# Summary and future

- **Collaboration between CPPM and IHEP was successful and fruitful in the past few years and will continue**

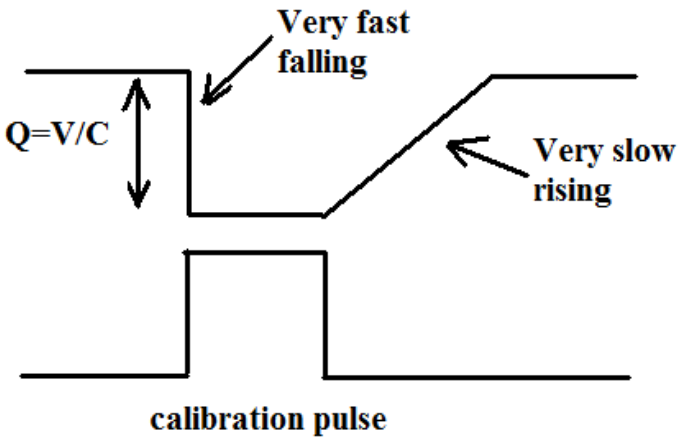
- **IHEP would like to contribute more on the coming ATLAS silicon pixel upgrades especially on the frond-end readout chips**

- **We are also eager to participate in CMS upgrade collaboration!**

# Thank you !

Backup Slides

# Functionality

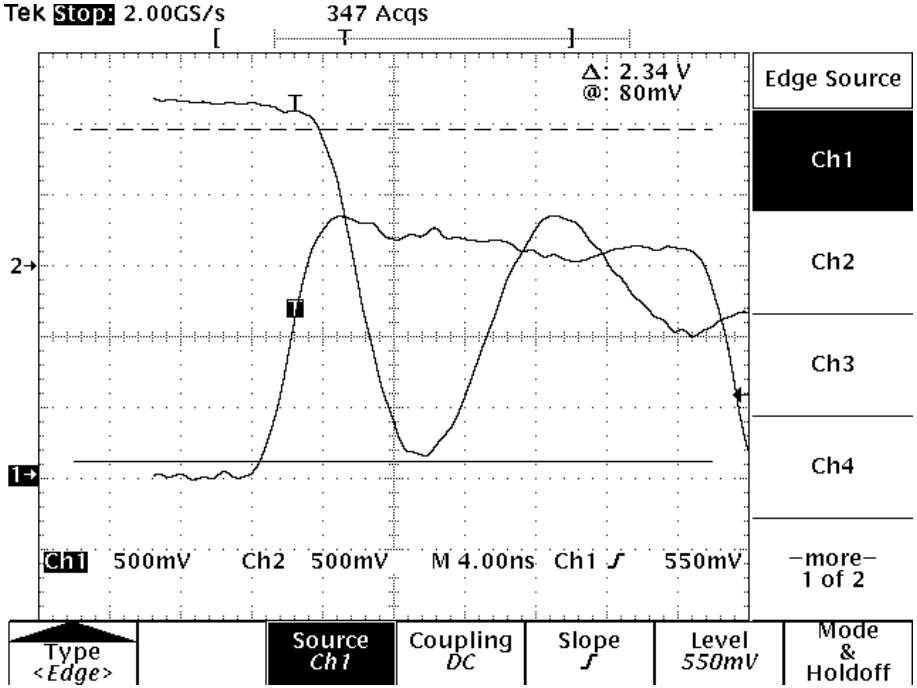



**Output specification:**

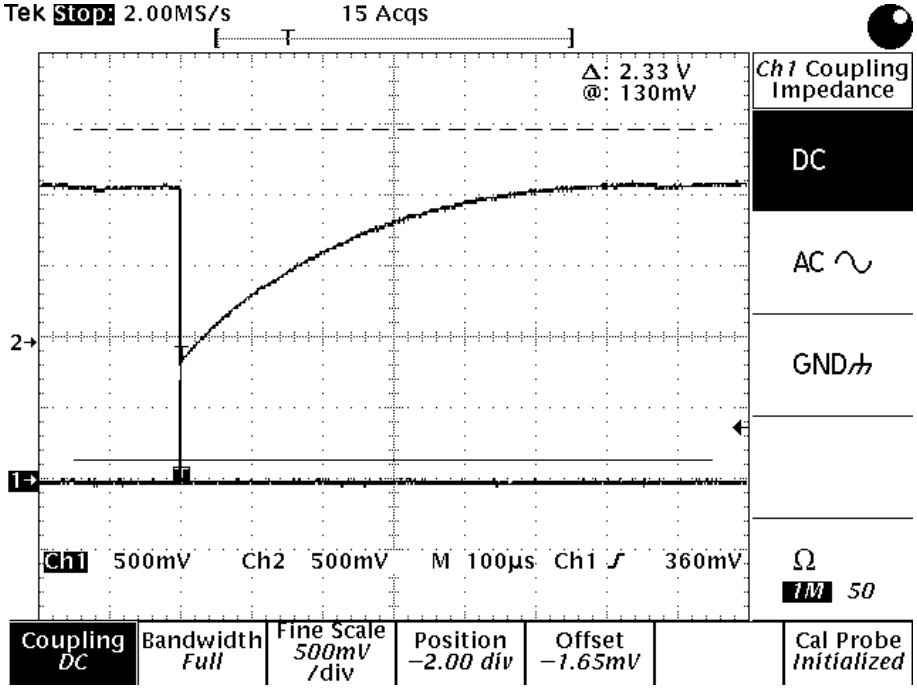
1. **Very fast falling edge -> charge injection (less than 2.5ns @ 0.5ns input rising edge)**
2. **Very slowing rising edge -> baseline restoration (3-bits tuning, 20 μs ~ 500 μs)**

**Ringings detected due to the unterminated cable**

**Expected to be eliminated if dwelled inside the chip**

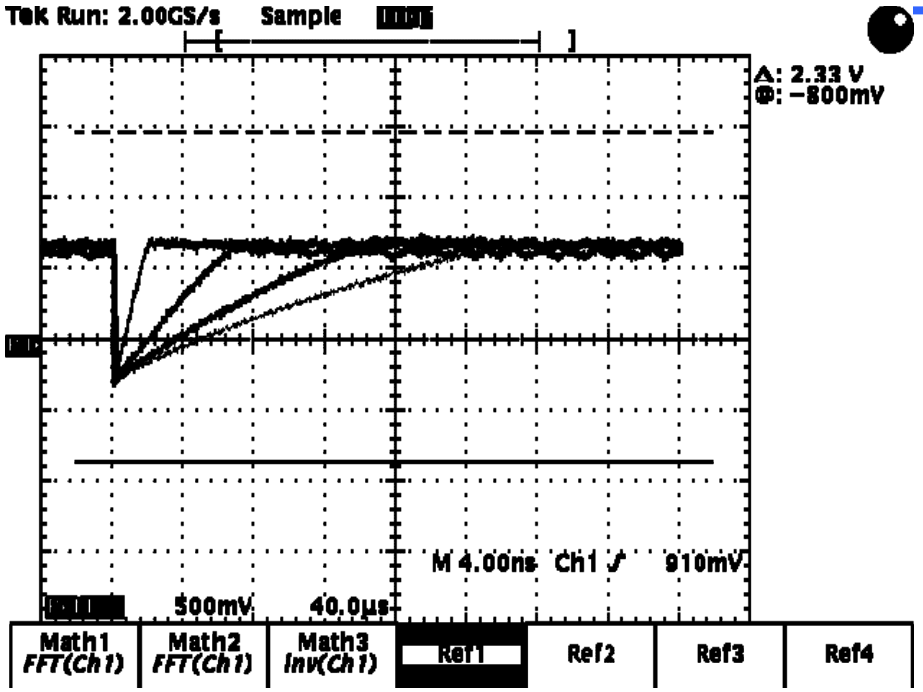



**falling edge ~ 4ns @ 2ns input rising edge**

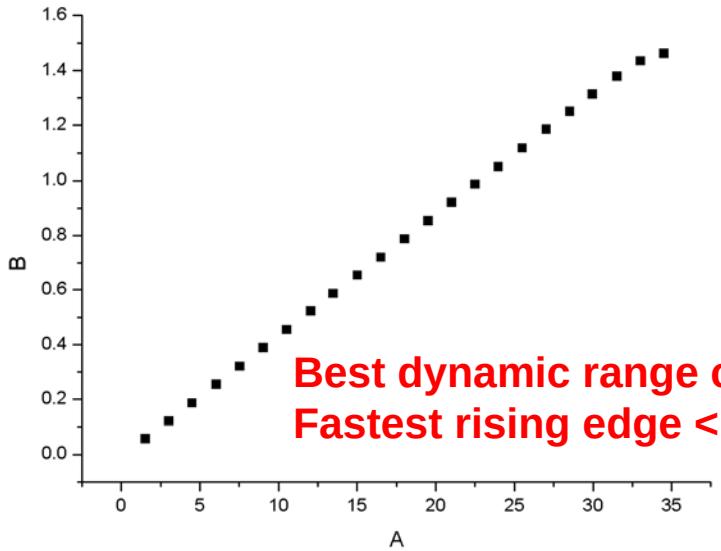


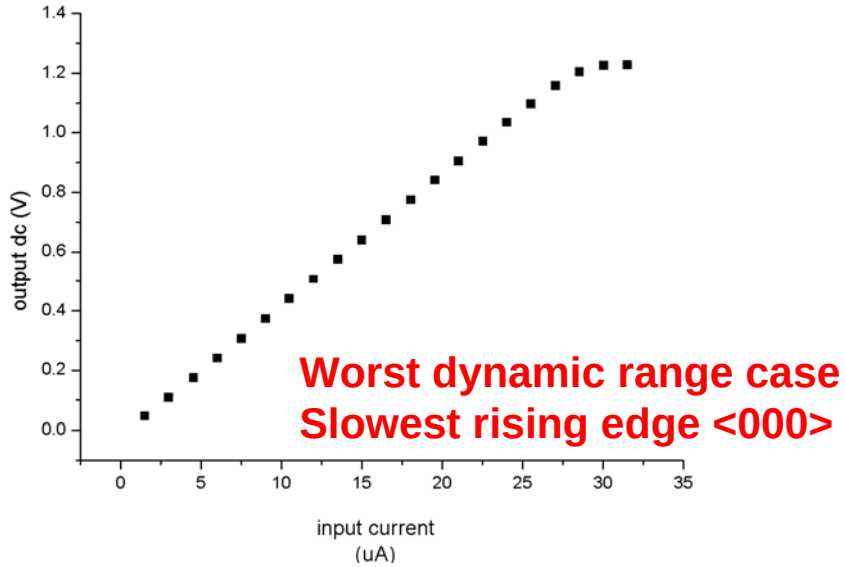

**Rising edge ~500 μs @ 25uA input current**

# Performance

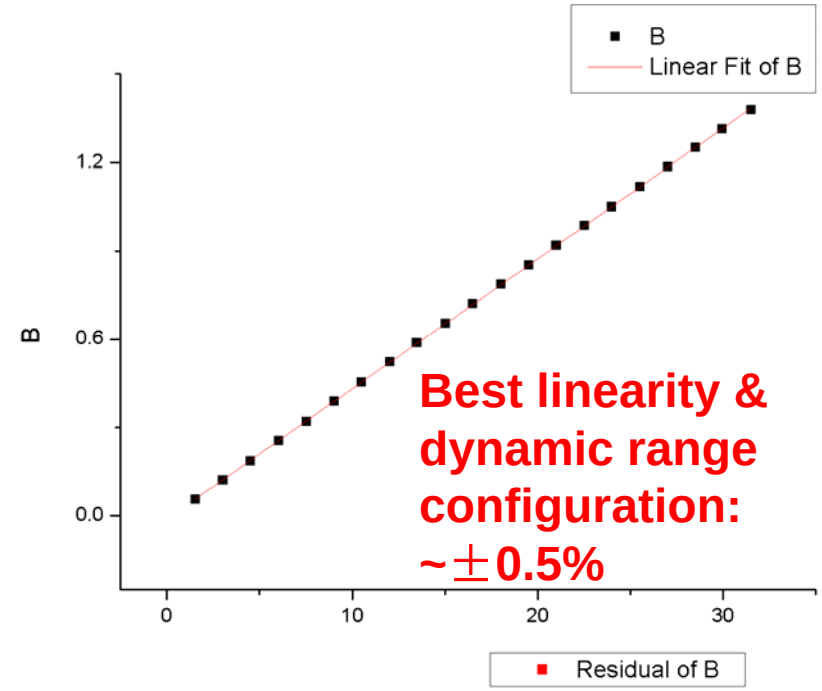



- **Rising time tuning:**
  - Overlapped snapshots from four measured outputs with different tuning bits configuration( 001/011/101/111)
  - Same input current 20 µA, output 1 V
  - Same time scale 40 µs/div
  - Showing rising time is tunable 20~400 µs
- **Dynamic range:**
  - Best case: fastest rising: 1.45 V
  - Worst case: slowest rising: 1.3 V
  - Same result as in simulation

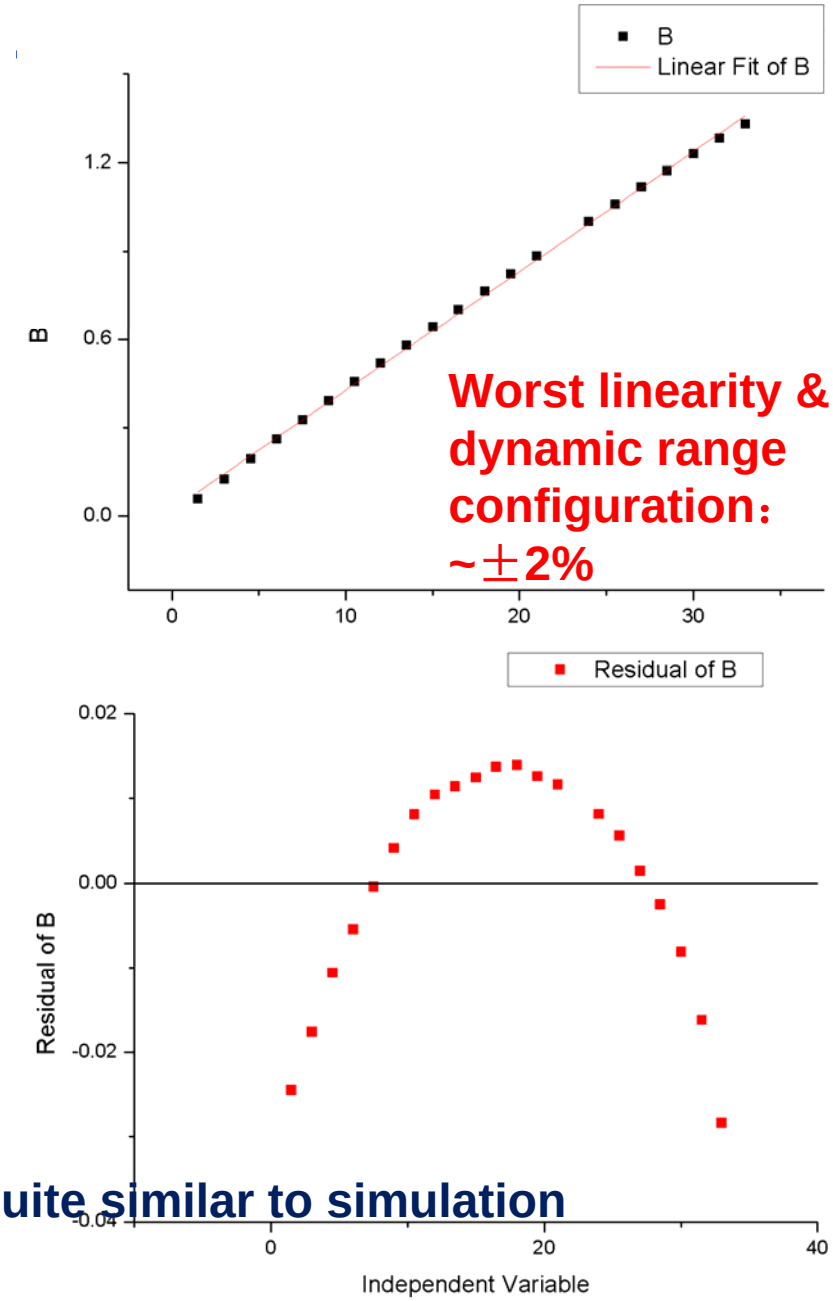


# Linear fit result



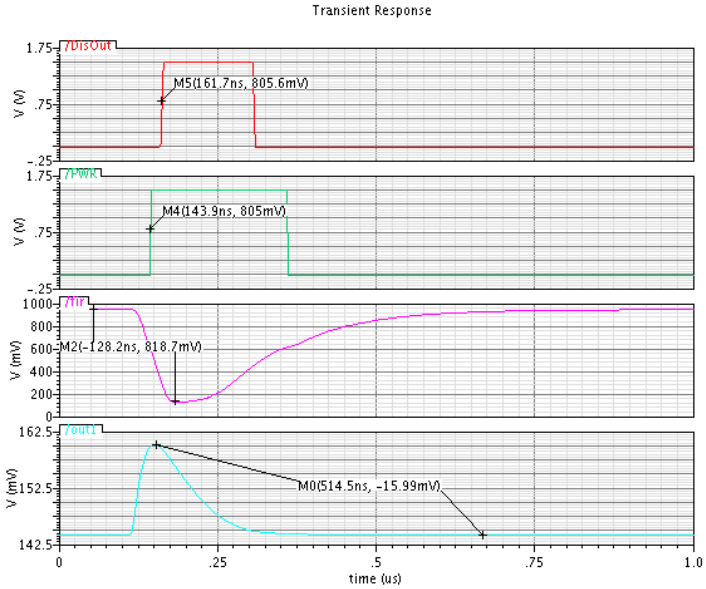

**Best linearity & dynamic range configuration: ~±0.5%**

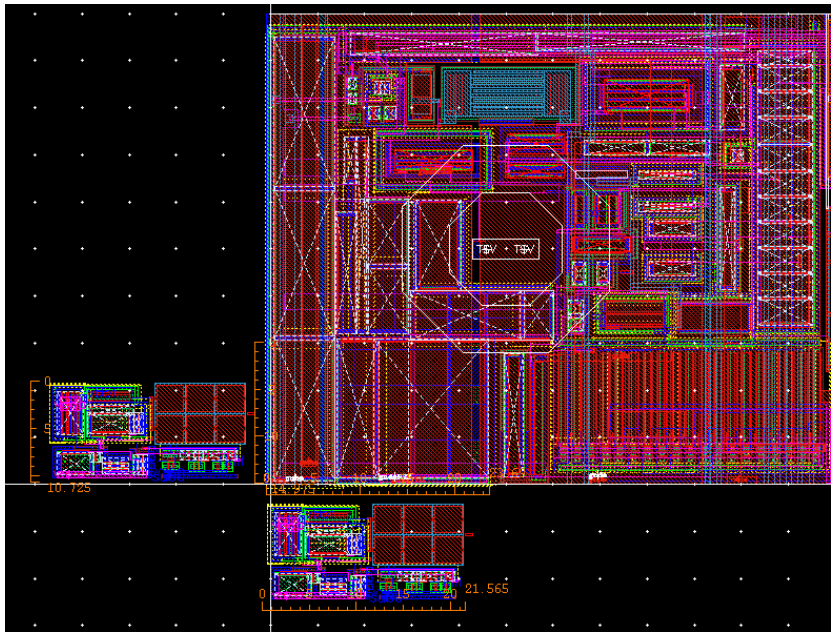
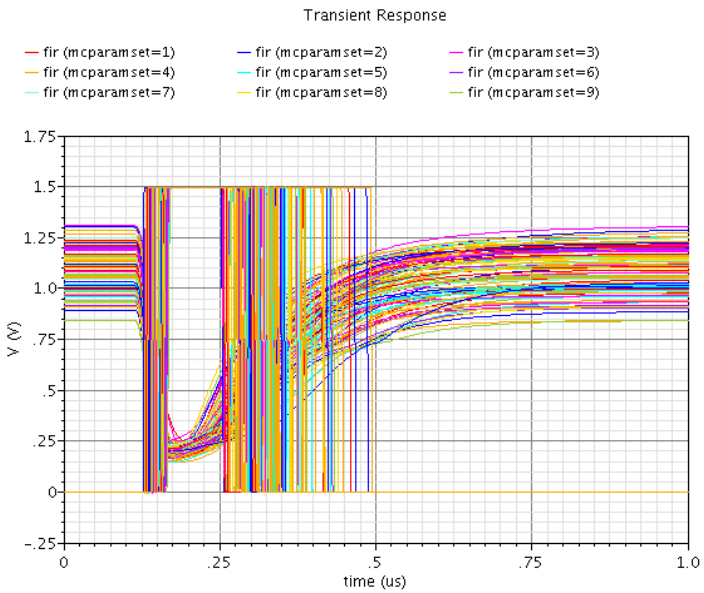



**Worst linearity & dynamic range configuration: ~±2%**

**Both results are quite similar to simulation**

# Design and simulation




- **Transimpedance**
- **Equivalent:**
  - **DC close loop (operating pt.)**
  - **AC open loop (large gain)**
- **Optimization: para. & corner**
- **Discriminator: modified for fast wakeup and settling**
- **M.C. sim: explore the full corner range**