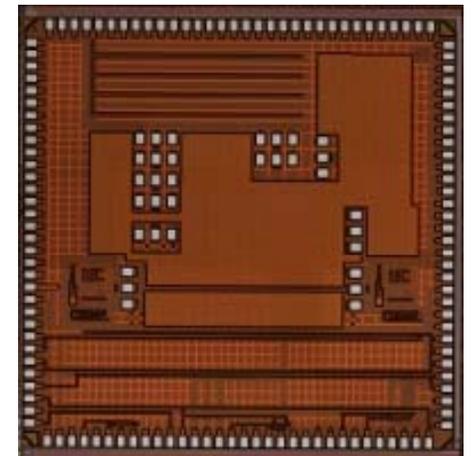
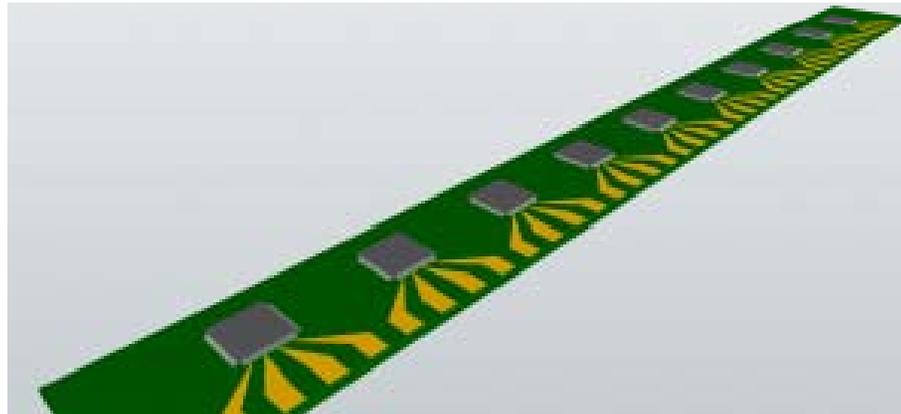


# Electronics Overview

Gary Varner for the LAPPD Electronics Group

Year 2 Progress and Plans for Year 3

20-MAY-2011 Electronics GPC Review



# Recommendation last gp summary: item 1

“It was not clear from the presentations how well the electronics development effort is integrated with other parts of the project. In particular, there may be interdependencies or requirements from other aspects of the project that could impact the electronics design, and it was not clear how this feedback and interaction are incorporated into the electronics design. The committee recommends that formal discussions with the various groups in the project be incorporated into electronics design process to ensure that there are no surprises during this second critical year, where the projects milestones show the development of an integrated device.”

- **Request interdependency of electronics design be clarified**
- **Suggest formal discussions with other groups**
- **Provide project milestones for an integrated device**

# Response to last gp summary: **item 1**

- **Request interdependency of electronics design be clarified**
- **Suggest formal discussions with other groups**
- **Provide project milestones for an integrated device**

**As a direct result of this recommendation there have been many more regular presentations at the regular Tuesday meeting. In addition, there has been much dialog and directly working together on items such as anode strip tests (Herve) and using prototype readout as part of characterization (Eric). Year 3 milestones that embody an integrated device will be presented today.**

# Recommendation last gp summary: item 2

“As a particular concern related to the above, it was not clear from the presentations how certain aspects of the electronics development meshes with the mechanical design. In particular, there were questions about the high voltage distribution inside of the photo-detector, signal flow and return paths, and the overall grounding scheme. Also, there were concerns about the sensitivity of the electronics to electrostatic discharge, such as sparks induced by high voltage. The committee recommends that the Electronics group and the Mechanical Group begin to develop a plan for how these two aspects of the project would be integrated to understand these issues, and to address any problems that might exist.”

- **Request interdependency of electronics design be clarified**
- **Request information on High voltage distribution plans**
- **Clarify signal and current return paths**
- **State plans to address discharge/sparking**

# Recommendation last gp summary: **item 2**

- **Request interdependency of electronics design be clarified**
- **Request information on High voltage distribution plans**
- **Clarify signal and current return paths**
- **State plans to address discharge/sparking**

**The high voltage distribution has been largely decoupled from the readout electronics effort. We expect experience with the first tiles to be invaluable and pick-up/noise issues shall manifest themselves. Signal and current return has been actively studied. ESD protection on the chip input will be augmented with additional, external protection.**

# Recommendation last gp summary: **item 3**

“There were no presentations on system aspects, such as global clock distribution in a large detector array, system synchronization, and error detection/error correction. In particular, there are concerns as to how the front-end chip would recover from either data transmission errors or synchronization problems. The committee recommends that these be considered soon, as there may be aspects that will concern the design of the front-end chip.”

- **Request readout architecture, timing and control be clarified**
- **Identify data transmission/synchronization errors that might impact ASIC design**

# Response to last gp summary: **item 3**

- **Request readout architecture, timing and control be clarified**
- **Identify data transmission/synchronization errors that might impact ASIC design**

**Mircea will present the current plan for the complete (beam test) readout system configuration. Worrying about some of these issues may be a bit premature, as we are still at an early prototype stage. Nothing in the design of the front-end ASIC precludes such synchronization and error detection, though that is envisioned to be largely the domain of the companion state-machine/event processing programmable logic.**

# Recommendation last gp summary: item 4

“There were no presentations on how the electronics would be calibrated, nor what aspects of the electronics will need to be calibrated. Some of the issues include identification of the corrections that might be needed, and how and where in the system they would be implemented. Several aspects discussed include time dependence corrections, amplitude dependence corrections, capacitor variations, clock phase corrections, etc. The committee recommends that the group begin to identify what kind of calibration techniques will be needed to address these, and how they might be incorporated into different levels of the data acquisition system. This plan should be a starting point, which evolves to include system issues, including the calibration of the physical detector, calibration of the front-end chips, and what role the back-end processing plays in the calibration process.”

- **Request Calibration procedures, constants and methods be presented**
- **Clarify a number of integrated system issues and items**

# Response to last gp summary: **item 4**

- **Request Calibration procedures, constants and methods be presented**
- **Clarify a number of integrated system issues and items**

**Kurtis has performed a number of calibration studies and will present a short synopsis of what constants and measurements are needed and the methodology to determine them. We have been exploring two paths for calibration/real-time correction and will present them today. Both use the same methodology.**

# Recommendation last gp summary: item 5

“Perhaps the most serious issue identified by the committee is the reversed stripline anode design. The signal attenuation at the end of the stripline is regarded as a serious concern. We are also concerned that impedance mismatch at the tile boundaries will cause reflection and/or attenuation of the signal. The group, along with Project Management, needs to resolve this issue soon, in case alternate strategies must be employed. In particular, a “conventional” stripline design might be needed, where the signal pick-off is on the inside of the plate, and signal pins would have to be inserted into the glass. This is a significant mechanical issue, which could impact the development schedule. We recommend that this be resolved soon.”

- **Request resolution of the reversed stripline anode design**
- **Clarify if signal pins through glass are needed, as this represents a significant risk**

# Response to last gp summary: **item 5**

- **Request resolution of the reversed stripline anode design**
- **Clarify if signal pins through glass are needed, as this represents a significant risk**

**The committee was right to be concerned and the problem is highly non-trivial. We believe sufficient tests of a balanced transmission line that addresses the mechanical issues have been made and will be presented today. Fermilab RF expert Dave McGinnis has been brought on-board to provide guidance in the studies, which have been made possible through new tools, such as the acquisition of a network analyzer, and new test benches.**

# Recommendation last gp summary: item 6

“While the testing of the front-end chip is progressing well, the proponents did not present plans for testing the electronics with an integrated photo-detector. The committee recommends that the Electronics Group, along with Project Management, begin to develop a plan for such testing. It is not too early to do so, given the Year 2 milestones that are looming. In particular, some of the relevant tests include measurement of quantum efficiency, overall gain, gain and readout uniformities transit time uniformity, rate dependencies, etc. It was not clear how the new electronics would be used to test these aspects of the integrated device, nor what resources would be needed to do so. In a related aspect, the committee recommends that the group develops a contingency plan for testing both the electronics and an integrated device. In the event that there are delays in the development of the MCP or the photocathode of the large-area device. This may require planning with the MCP and Photocathode groups.”

- **Request developing a testing plan in concert with Project Management**
- **Clarification on testing dependence on electronics availability**
- **Provide contingency plans in the event of delays in other parts of the LAPPD project**

# Response to last gp summary: **item 6**

- Request developing a testing plan in concert with Project Management
- Clarification on testing dependence on electronics availability
- Provide contingency plans in the event of delays in other parts of the LAPPD project

The Project Management is keenly aware that testing with PSEC3 has just begun and having a working tile is an essential next step. Some of the integration and system performance items raised are beyond the scope of this group, though we are working with the relevant groups to provide supporting electronics for upcoming tests. Both test (eval) and full anode strip readout boards have been developed and will be capable of using multiple ASICs (PSEC4, IRS2, BLAB3A), increasing flexibility.

# Recommendation last gp summary: **item 7**

“The committee is concerned that the electronics development does not have sufficient manpower resources to meet the Year 2 milestones and going forward. In particular, the areas identified that could benefit from additional resources include firmware development, software development, back-end design (DAQ), and overall system design. We recommend that additional resources be brought into the group, including students, postdocs, and engineers. The LAPPD project should also consider the addition of a system engineer to oversee the interfaces between different groups in the project.”

- **Request additional resources be made available to provide the engineering and test support required to fulfill stated milestones**

# Recommendation last gp summary: **item 7**

- **Request additional resources be made available to provide the engineering and test support required to fulfill stated milestones**

**While the group size has not increased, we have been very efficient with available manpower resources. We agree that a system engineer would be quite helpful, to coordinate the efforts. However this is really a question of available resources.**

**We have been proactive in addressing this point and since the last review 2 major, multi-year proposals have been submitted to provide significant, supplemental funding directly to UC and Hawai'i to address these manpower needs. Should both of these be unsuccessful, we are considering pursuing DOE support directly for the UC and Hawai'i efforts.**

# Recommendation last gp summary: **item 8**

“The committee was very impressed with progress made with the design and development of the PSEC chip. While the development appears to be proceeding well, the proponents presented contingency scenarios for using other sampling chips in the event that the PSEC development has problems or would not be ready in time to meet Year 2 milestones. The committee recommends that the Electronics Group work with Project Management to identify a point in time when a decision will be made regarding which chip to go forward with to meet project milestones. That point would have to be within the next 3-6 months in order to be ready for test beam tests by the end of Year 2.”

- **Clarify with Project Management the role of the PSEC development, alternatives and what to be use in further testing and beam tests**

# Response to last gp summary: **item 8**

- **Clarify with Project Management the role of the PSEC development, alternatives and what to be use in further testing and beam tests**

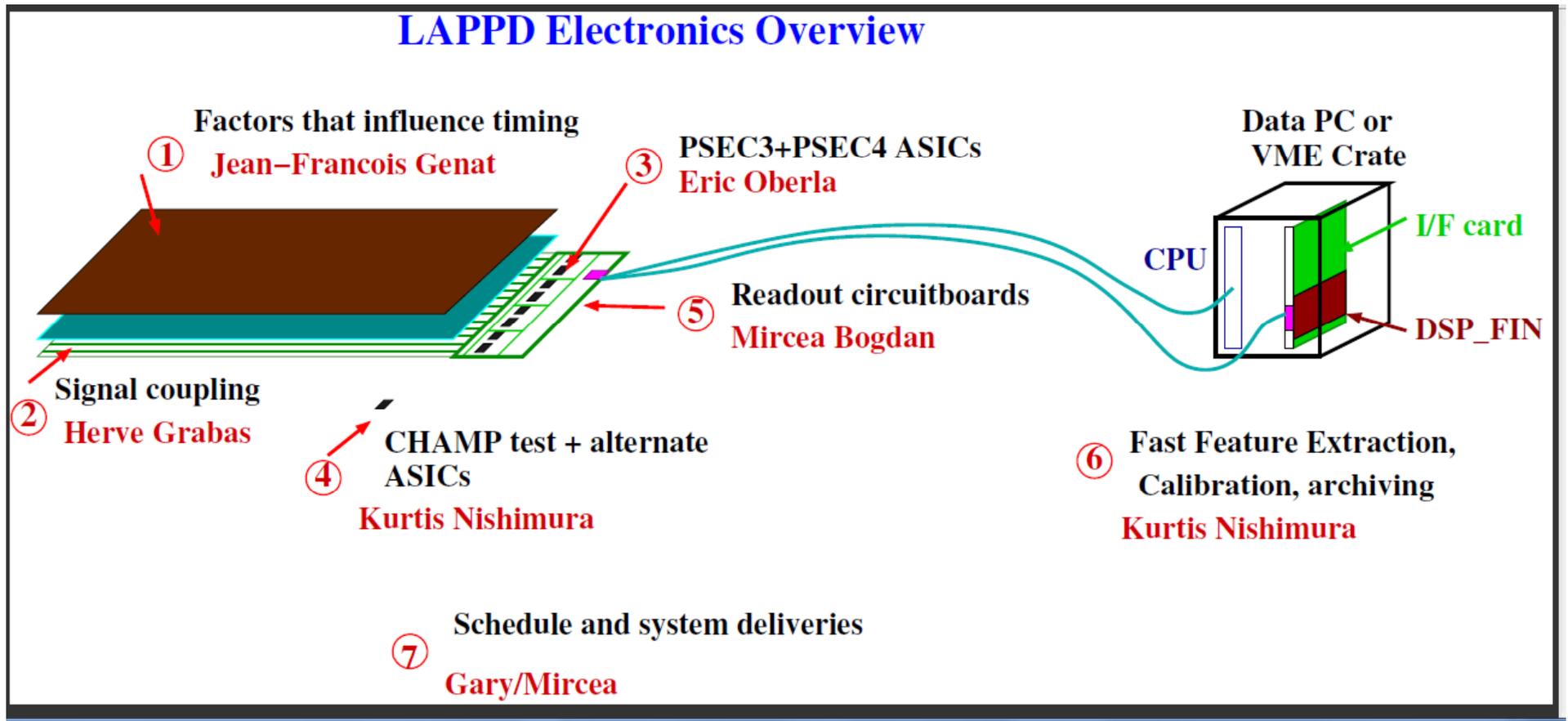
**It has been made clear with Project Management that PSEC4 is our baseline ASIC. Given that it is a very conservative set of corrections to PSEC3, we have confidence it will be useable for the next round of testing.**

**The alternate ASICs presented continue as fall-back options, should this not be true, and also applications where a longer sampling depth, longer trigger latency, electronics gain, or some other project-specific requirement is needed. The electronics is modular and can accommodate different ASIC options with little additional effort.**

# Some highlights since last review

1. Further understanding of the processes that limit timing resolution  
[http://psec.uchicago.edu/workshops/fast\\_timing\\_conf\\_2011](http://psec.uchicago.edu/workshops/fast_timing_conf_2011)
2. A much more fundamental understanding of how to couple the charge signal into the readout anodes
3. Understanding how to make a electrically and mechanically viable readout
4. First and impressive test results with the PSEC3 and submission of PSEC4, to clean up a few, minor bugs
5. Expanded significantly expertise with the IBM 130nm process and tested future subcircuits on the CHAMP ASIC
6. Fabrication of ASIC evaluation boards, as well as the first tile/module scale readout boards
7. Exploration of options for large-scale/high-speed readout, with a number of viable solutions identified
8. Evaluation of calibration procedures, required constants, and data archiving

# LAPPD Electronics Overview



Initial systems all based on USB readout  
Giga-bit fiber Tx/Rx for high rate/throughput

# LAPPD Electronics and Integration Godparent Review

Friday 20 May 2011  
from 08:00 to 18:00UTC  
at Argonne National  
Laboratory ( Bldg 360, Rm  
A224 )

[Friday 20 May 2011](#) |

Friday 20 May 2011

[top](#)↑

08:00

Morning Refreshment

08:30	   Welcome (05')	Zikri Yusof
08:35	  Electronics Overview (30')  Slides  )	Gary Varner
09:05	  Review/update on physical parameters that influence timing (20')	Jean-Francois Genat
09:25	  Signal development and coupling to Readout Electronics (20')	Herve Grabas
09:45	  The PSEC3 and PSEC4 ASICs (30')	Eric Oberla
10:15	Break	
10:30	  CHAMP lessons and alternative ASIC options (20')	Kurtis Nishimura
10:50	  Readout System Overview (20')	Mirocea Bogdan
11:10	  Data processing, Calibration and archiving (30')	Kurtis Nishimura
11:40	  System Deliveries and Testing (20')	Eric Oberla
12:00	  Schedule and Plans (30')	Mirocea Bogdan/Gary Varner
12:30	  Open questions (15')	
12:45	Lunch	
13:45	  Open discussion (if necessary) (30')	
14:15	  Godparent Committee Discussion/Draft of Report (30')	